$Si{:}SrTiO_3$-Al_2O_3-$Si{:}SrTiO_3$ multi-dielectric architecture for metal-insulator-metal capacitor applications

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Abstract

Metal-insulator-metal (MIM) capacitors comprised of amorphous $Si{:}SrTiO_3$-Al_2O_3-$Si{:}SrTiO_3$ multi-dielectric architecture have been fabricated employing a combination of pulsed laser and atomic layer deposition techniques. The voltage linearity, temperature coefficients of capacitance, dielectric and electrical properties upon thickness were studied under a wide range of temperature (200 – 400 K) and electric field stress (± 1.5 MV/cm). A high capacitance density of 31 fF/μm^2, a low voltage coefficient of capacitance of 363 ppm/V^2, a low temperature coefficient of capacitance of < 644 ppm/K and an effective dielectric constant of ~133 are demonstrated in a MIM capacitor with ~1.4 nm capacitance equivalent thickness in a ~40 nm thick ultra high-k multi-dielectric stack. All of these properties make this dielectric architecture of interest for next generation highly scaled MIM capacitor applications.

Metal-insulator-metal (MIM) capacitor structures, utilizing high-k materials having high dielectric constant and low dissipation factor, as charge storage and noise reduction media for adequate storage capacitance with reduced feature size (equivalent scaling) have attracted the interest of researchers due to their potential applications in dynamic random access memory

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(DRAM), radio-frequency (RF) and mixed signal capacitors.[1] The oxides and nitrides of silicon possess good voltage linearity and low temperature coefficients. However, due to their low dielectric constants, capacitance density achieved will be normally low.[2] Capacitance densities could be raised by reducing the dielectric thickness, which also achieves better device miniaturization and reduces overall device cost. However, this will create the problem of poor voltage linearity and large leakage current. Several high-k materials[3,4,5] have been studied for MIM capacitor applications, but it has been challenging to satisfy all performance requirements[6] with a single dielectric material. Great efforts have been going on to design/engineer MIM capacitor architectures with improved voltage linearity, low leakage current and high electric field strength using appropriate combination of materials with higher (lower) permittivity and lower (higher) bandgap.[7]

$SrTiO_3$ (STO) has been the most studied perovskite dielectric, offering high dielectric constant >100 (ultra high-k) even in the form of ultra-thin layers.[8] Along with a low bandgap of 3.2 eV, it has a paraelectric phase above 105 K.[9,10] However, crystalline layers of STO suffer from high leakage current densities originating from the grain boundary channel as well as a decreased metal/insulator barrier height due to its inherent low bandgap. These problems can be solved by using an STO layer in its amorphous phase and by stacking it with large-bandgap materials (e. g., Al_2O_3, SiO_2, MgO etc.) in multi-dielectric structures.[11] Al_2O_3 exhibits a large bandgap of 8.7 eV with a low dielectric constant of ~9 and possesses high electric field strength and low oxygen diffusivity, along with good thermal stability.[12] $SrSi_{0.03}Ti_{0.97}O_3$ (SSTO) developed in our laboratory has a lower bandgap of 3.3 eV with higher dielectric constant of ~300 in polycrystalline ceramic form.[13] Thus a multi-dielectric SSTO/Al_2O_3/SSTO (SAS) stack formed by incorporating an ultra-thin barrier layer of Al_2O_3 between SSTO thin layers can

improve the leakage characteristics and enhance the breakdown voltages by trapping the charge carrier flow at the dielectric interfaces without pronounced effective permittivity reduction and can be a good candidate for MIM capacitor applications. Also the silicon doping in STO may improve its voltage linearity. This is due to the fact that the SSTO solid solution matrix will have an effective/compensating polarization which is the resultant of negative curvature capacitance-voltage (C-V) in SiO_2 (with -α, voltage coefficient of capacitance, originating from orientation polarization) and positive curvature C-V in STO (with +α originating from electrode/ionic polarization, carrier injection, or electrostriction).[14,15,3] A similar compensating feature is expected in the case of temperature coefficient of capacitance (TCC), since STO possesses a positive value[16] whereas SiO_2 has a negative value.[17]

In this work SAS dielectric stacks of different thicknesses with a monolayer of Al_2O_3 sandwiched between SSTO layers were investigated to achieve better performing MIM capacitors with higher capacitance density, lower voltage coefficient of capacitance and controlled leakage current. The stacks were studied under a wide temperature range (200 – 400 K) and electric field stress (± 1.5 MV/cm) to check their robust performance in extreme operating environmental conditions, such as in automotive, military, and aerospace applications, in addition to mainstream consumer and office applications.

SSTO thin films were pulsed-laser-deposited (PLD) on commercially available $Pt/TiO_2/SiO_2/Si$ substrates maintained at a temperature of 300 °C at an ambient oxygen partial pressure of 10 mTorr by a two-stage process. First, a SSTO ceramic target was ablated by a KrF excimer laser beam (248 nm, 10 Hz) of energy density ~1.2 J/cm^2 after passing it through a beam-shaping aperture to fabricate the first SSTO layer at a growth rate of ~1 Å/pulse. The Pt substrate was positioned on the resistively heated stage at a distance of 5 cm from the ceramic

target. Second, a monolayer of Al_2O_3 (~4 Å thin to keep the capacitance density of the stack high) was coated on the PLD-deposited films by plasma-enhanced atomic layer deposition (PE-ALD) utilizing a Picosun R150 system. 3 cycles of PE-ALD at a self-limited growth rate of ~1.3 Å/cycle were carried out for the Al_2O_3 thickness of ~4 Å. Trimethyl aluminum (TMA) and oxygen plasma were used as the metal precursor and oxidant for Al_2O_3 deposition. The substrate temperature was kept at 200 °C. Finally the SSTO layer deposition was repeated. Hence the final geometry of the tri-layer samples was a sandwich of SSTO (PLD-deposited)/Al_2O_3 (ALD-deposited)/SSTO (PLD-deposited) with total thicknesses of ~40, ~65, ~100 and ~190 nm. Thickness of the films was measured by stylus profilometry and later confirmed by analyzing the SEM cross-section images, as shown in Fig. S1 (a-d) in the supplementary material. The presence of Al in the film was confirmed by EDX, as shown in Fig. S1 (e). Disordered phase formation of the samples was checked in a slow scan mode (0.25 ^{o}/min) with a Rigaku Ultima III x-ray diffractometer (XRD) equipped with a CuK_{α} radiation (λ=1.5405 Å) source operating in Bragg-Brentano (θ-2θ) geometry at 40 kV and 40 mA. Pt metal top electrodes of thickness ~60 nm and diameter ~90 μm were deposited on the tri-layer stack by room temperature dc-magnetron sputtering (power density ~1 W/cm^2) through a metal shadow mask. Hence our final heterostructure stack is Pt/SSTO/Al_2O_3/SSTO/Pt, the schematic diagram of which is illustrated in Fig. S1 (f). The as-prepared MIM stacks were then annealed at 400 °C for 20 min in oxygen ambient for proper adhesion of electrodes and to recover from any possible sputter damage. All processes were carried out at temperatures $\leq$ 400 °C in order to meet the thermal budget requirement for back-end applications. The dielectric characterization and dc leakage current measurements were carried out under a vacuum of ~10^{-6} Torr, utilizing an HP4294A impedance analyzer and a Keithley electrometer (model #6517A). The samples were kept in the dark during

dielectric characterization. Temperature control (200–400 K) was achieved using a programmable Joule-Thomson refrigerator system [MMR Technologies].

X-Ray diffraction measurement was carried out on all thin-film stacks. Figure S2 shows the XRD pattern of the platinum substrate and that of the thickest stack (190 nm). No Bragg peak was observed from the tri-layer geometry except those from the substrate (i.e., Pt/TiO_2/SiO_2/Si), which confirms the amorphous phase formation of the dielectric stack. The AFM plan views of the films are shown in the inset (a-d) of Fig. S2 in order of increasing thickness (40, 65, 100 and 190 nm). Root mean square (r.m.s.) roughness of 3.59, 3.94, 4.37 and 4.03 nm were obtained for the films of thickness 40, 65, 100 and 190 nm. It can be seen that the film with the lowest thickness has the finest morphology features. The change in morphology might be due to particle incorporation, an inherent shortcoming of PLD.

Figure 1 shows the scaling of capacitance density for four capacitance equivalent thickness (CET) values at three different temperatures (200, 300 and 400 K) measured at zero bias voltage. The capacitance density for the lowest CET value (1.4 nm) was obtained as 29 fF/µm^2, 31 fF/µm^2 and 32 fF/µm^2 and that for the highest CET value (6.6 nm) was found to be 5 fF/µm^2, 6 fF/µm^2 and 7 fF/µm^2 at temperatures 200, 300 and 400 K. The capacitance density was greater than 10 fF/µm^2 for the three stacks with CET values 1.4 nm, 2.4 nm, and 4.2 nm, which meets the ITRS requirement for the year 2018.[18] In all the capacitors the capacitance density was found to vary in a fairly linear manner with respect to temperature (Class 1).[19] The temperature coefficient of capacitance α_T, a figure of merit of the dielectric capacitor devices, is formulated as:

$$\alpha_T = \frac{C_T - C_{RT}}{C_{RT}(T - T_{RT})} \times 10^6 \text{ ppm/K} \quad (1)$$

where C_T and C_{RT} are the capacitance values at a particular temperature limit T and at room temperature (T_{RT} = 300 K). The numerical values of α_T for the sample with the lowest CET of 1.4 nm were determined to be 644 and 220 ppm/K at the extreme temperatures 200 and 400 K, respectively, at 100 kHz ac signal frequency and are within the 750 ppm/K limit set by the Electronic Industries Alliance (EIA). The capacitance density versus temperature plot [inset (a) of Fig. 1] provided a positive slope of 1.35×10^{-2} fF/μm^2 K. An elevation in capacitance was observed with decreasing frequency at zero bias voltage and at 300 K for all film thicknesses, as shown in the inset (b) of Fig. 1. The reasons behind this may be the bottom electrode resistivity, relaxation of free carriers and dipoles (nonlinear Kerr effect), and/or a lossy interfacial layer.[20] Another contributing influence might be the effect of fewer charge traps at the interface; these cannot follow the signal at higher frequencies.

An important parameter of a MIM capacitor for RF and AMS applications is its capacitance voltage linearity – the dependence of capacitance C on the dc bias V.[3] The voltage linearity of MIM capacitors is modeled with a second-order polynomial equation,

$$\frac{\Delta C}{C_0} = \frac{C_v - C_0}{C_0} = \alpha V^2 + \beta V , \quad (2)$$

where V is applied bias voltage; C_v, the capacitance at a particular voltage; C_0, the zero-bias capacitance; α and β, the quadratic and linear voltage coefficients, expressed in units of parts per million (ppm)/V^2 and ppm/V, respectively; and $\Delta C / C_0$ is the normalized capacitance. α, also known as voltage coefficient of capacitance (VCC), represents the stability of the capacitor and is a more relevant parameter to be minimized. Its value should be within 100-1000 ppm/V^2 for RF and AMS device applications.[21] A positive value of α indicates the rise in capacitance

density with applied voltage, which may be ascribed to the high degree of electric field polarization.[1,22,23] The capacitance values were measured with voltage sweep from -5 V to +5 V at temperatures 200 K, 300 K, and 400 K and at the frequencies of 10 kHz, 100 kHz and 1 MHz.

Figure 2 shows the variation in VCC with CET at an ac signal frequency of 100 kHz for three different temperatures measured at zero bias voltage. The normalized capacitance vs electric field (± 1.5 MV/cm) plots recorded at different temperatures for CET value 1.4 nm are shown in the inset (a) of Fig. 2 (as an example). The nearly symmetric curves at 200 and 300 K may have originated from dielectric bulk properties like ion polarization or electrostriction,[24] whereas the appearance of asymmetry in the curve at 400 K can be attributed to the dominant electrode polarization.[25] The maximum VCC value obtained was ~363 ppm/V^2 for CET value of 1.4 nm; and the minimum VCC was ~10 ppm/V^2 for CET value of 6.6 nm at ambient conditions, which are quite low values. α and β values obtained for all four films at various temperatures and frequencies are summarized in Table S1. In all the dielectric stacks α was found to be less sensitive with respect to temperature and did not follow the usual direct proportionality with temperature.

The obtained higher (lower) VCC at lower (higher) CET value indicates that the capacitance of the insulator stack has a moderate voltage dependence upon dielectric thickness,[26] which is clear from Fig. 2 and Table S1. The result in Fig. 2 (b) and Table S1 shows that VCC rises with frequency decrease, showing a dispersive behavior which might be due to bulk-dielectric traps near the SSTO/Pt interface. With increasing frequency, the trapped-charged-induced dipoles and the excess mobile charges can hardly follow the ac signal, due to their longer relaxation times; this results in decreased carrier mobility and hence smaller VCC.[23,2,27] The bias-polarity-

independent normalized capacitance plots (inset (a) of Fig. 2) indicate similar time constants for the traps at both the dielectric/electrode interfaces.

At any given frequency we observed an increase in VCC with reduction in thickness (Table S1). This can be explained by the direct proportionality between relaxation cut-off frequency and conductivity.[28] Extrinsic effects can originate from space-charge relaxation mechanisms such as electrode polarization,[3,29] implying that thinner films should have higher conductivity, causing higher leakage current. This is true in our study, as shown in the inset (b) of Fig. 4. Equation (2) involves the relationship $\alpha \propto t^{-2}$, between α and t.[30] Plotting the room-temperature quadratic voltage coefficient as a function of CET (as shown in Fig. S4), a good agreement with this inverse square relation was obtained for 100 kHz data, with an estimated exponent equal to 2.15. This exponent x was obtained as 1.98 and 1.91 at 200 K and 400 K, respectively, at the same ac signal frequency of 100 kHz (Fig. S4). The strong thickness dependence of α shown in Table S1 is in accord with the higher value of x obtained for these stacks.

Figure 3 (a) shows the variation in effective dielectric constant for the four SAS stacks in the frequency range of 100 Hz to 1 MHz at room temperature. The dielectric constant showed a slight increase (from 133 to 143 at 100 kHz) with increase in thickness (from 40 to 190 nm) as the thickness ratio of Al_2O_3 ($\varepsilon_r = 9$) layer to the total stack thickness is reduced. The observed decrease in permittivity with increase in frequency indicates that there is large dispersion due to Maxwell–Wagner type interfacial polarization. Electric dipoles are unable to be in phase with the frequency of the applied electric field, causing the dispersion,[31] which is in agreement with Koop's phenomenological theory.[32] The variation in dielectric constant with thickness at different temperatures is shown in the Fig. 3 (b). For all film thicknesses the dielectric constant was found to be decreasing with decrease in temperature.

A good understanding of the charge transport phenomena in these stacks is essential for the best operation and reliability of devices based on them. The temperature dependence of current density versus electric field for the stack having a CET value of 2.4 nm is shown in Fig. 4. A semiconductor behavior was observed. To model the conduction mechanism at room temperature, dc leakage data were re-plotted in Schottky coordinates (ln J/T^2 versus $E^{1/2}$), as shown in the inset (a) of Fig. 4. The expression for Schottky charge transport mechanism is given by,

$$J = AT^2 \exp\left[\frac{-q\phi_B}{kT} - \beta E^{1/2}\right], \text{ where } \beta = \frac{1}{kT}\left[\frac{q^3}{\alpha\pi\varepsilon_0\varepsilon_\infty}\right]^{1/2} \quad (3)$$

where A is the Richardson constant; T, absolute temperature; E, applied electric field; k, the Boltzmann constant; ϕ_B, the barrier height; ε_0, the permittivity of free space; and ε_∞, the electronic permittivity. The coefficient α is 4 for Schottky emission. The room-temperature Schottky plot can be approximated by a straight line and is indicative of electrode/interface-limited Schottky charge transport due to field-assisted thermionic emission of electrons over a barrier height ϕ_B. The numerical value of ε_∞ was obtained as 4.0 for the dielectric medium from the slope of the plot. Hence the long wavelength refractive index, n_∞ was determined to be 2.0 using the relation $\varepsilon_\infty = n_\infty^2$, which is comparable with the refractive index value of $SrTiO_3$ reported elsewhere using optical studies.[10] The barrier height at the SSTO/Pt interface estimated from the intercept of the linear fit of the Schottky plot was 0.74 eV and is in fairly good agreement with the value of 1 eV reported at $SrTiO_3$/Pt interface by Abe *et al*. The inset (b) of Fig. 4 demonstrates the leakage current increase with thickness reduction of the dielectric stack recorded at room temperature and at 1 V. The average breakdown field (E_{BD}) obtained for the

stacks was ~2 MV/cm, which gives a very high equivalent breakdown field [$Equivalent\ field = (E_{BD} \times k)/3.9$] of ~68 MV/cm by considering the permittivity (k) of the dielectric stack as 133. In these multi-dielectric stacks the breakdown electric field strength achieved is rather high, partially due to one dimension being at nanoscale, which allows a better heat dissipation and decreases the probability of finding critical defect concentrations.

In summary, MIM capacitors with a multi-dielectric architecture comprised of ALD-PLD grown amorphous Al_2O_3 and ultra high-k Si:$SrTiO_3$ layers have been fabricated and their voltage linearity, temperature coefficients of capacitance, dielectric and electrical properties investigated under harsh temperature (200 – 400 K) and electric field (± 1.5 MV/cm) conditions. The device with the lowest CET of ~1.4 nm yielded a large capacitance density of 31 fF/μm^2, a low VCC of 363 ppm/V^2, a low TCC of < 644 ppm/K and an effective dielectric constant of ~133. The dispersion in VCC with frequency and thickness variation was well characterized. DC leakage analysis implied Schottky emission as the dominant physical origin of current transport during carrier injection. All these results revealed that SAS is a suitable multi-dielectric architecture for future generations of highly integrated MIM devices.

Supplementary Material

See supplementary material for XRD, SEM, EDX, AFM, VCC data of the studied MIM stacks.

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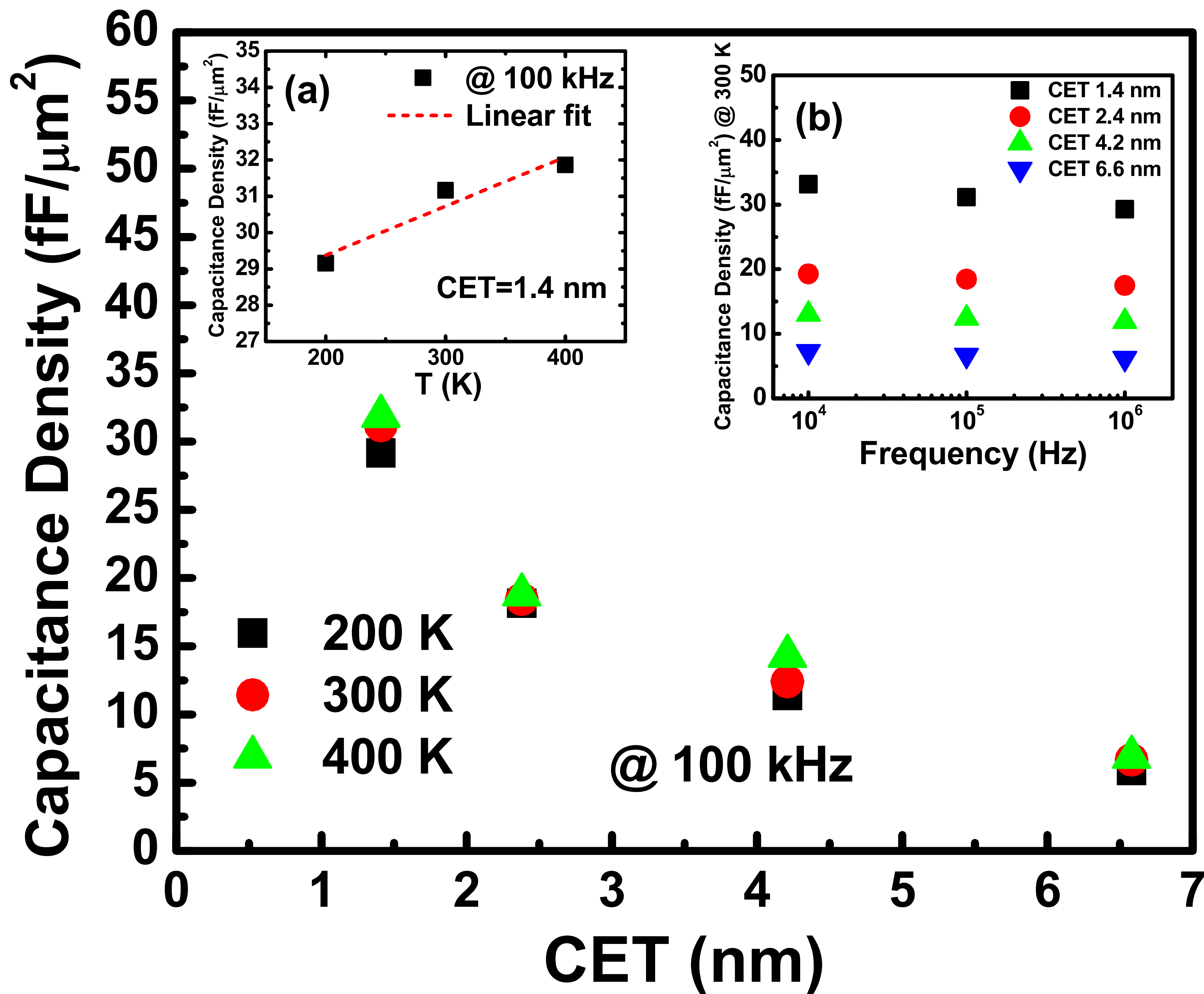
Figure Captions

FIG. 1. Variation of capacitance density with equivalent thickness (CET) at temperatures 200, 300 and 400 K measured at 100 kHz. Inset (a) shows a representative variation in capacitance density with temperature. The frequency dependence of capacitance density of four film stacks is given in the inset (b).

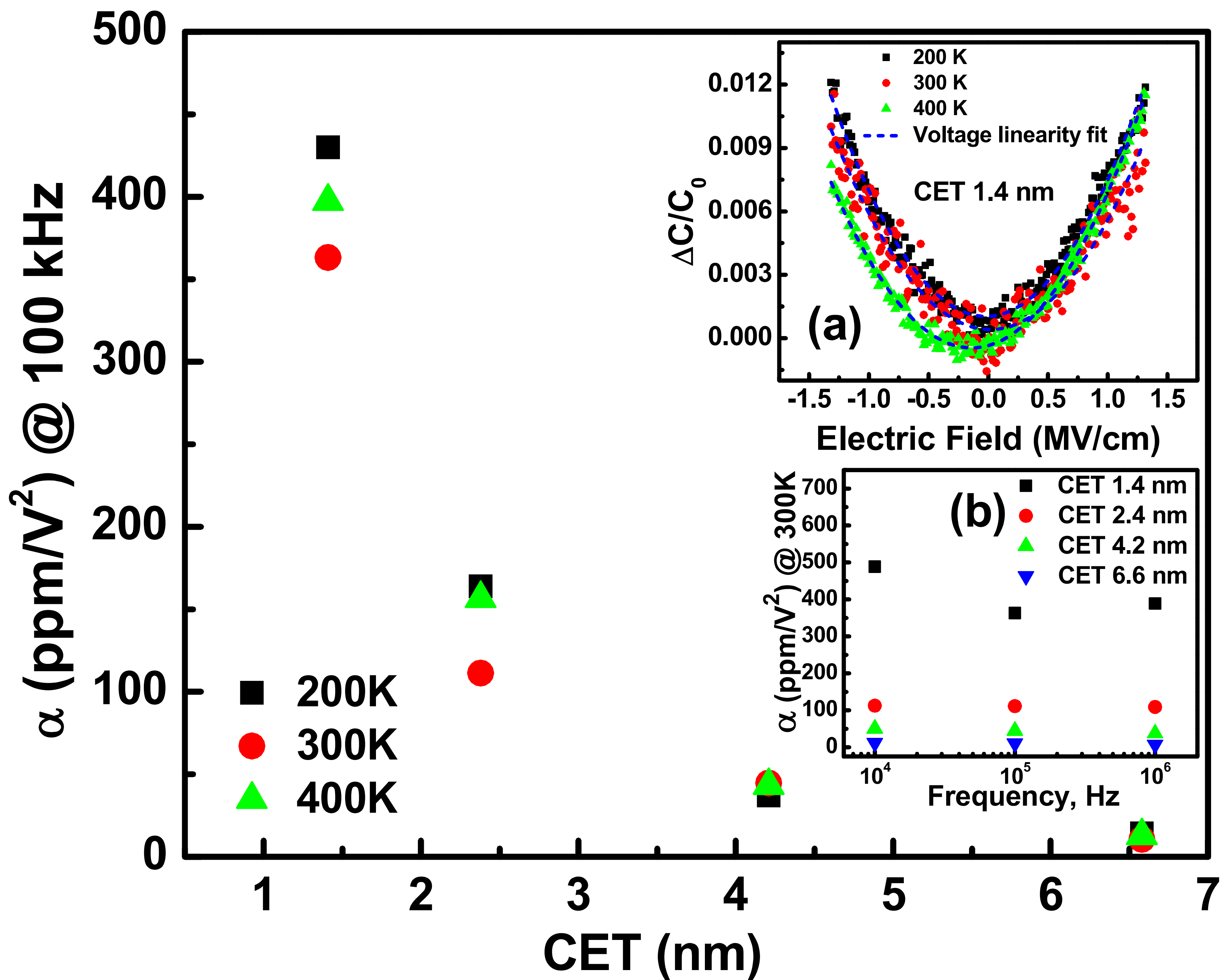
FIG. 2. Variation in VCC (α) with CET at zero bias measured at 100 kHz. a) Normalized voltage-dependent capacitance of 40-nm thick film at different temperatures. b) Frequency dependence of room temperature VCC (α) for four CET values.

FIG. 3. (a) Variation of dielectric constant with frequency and (b) Thickness dependence of dielectric constant at three different temperatures measured at 100 kHz.

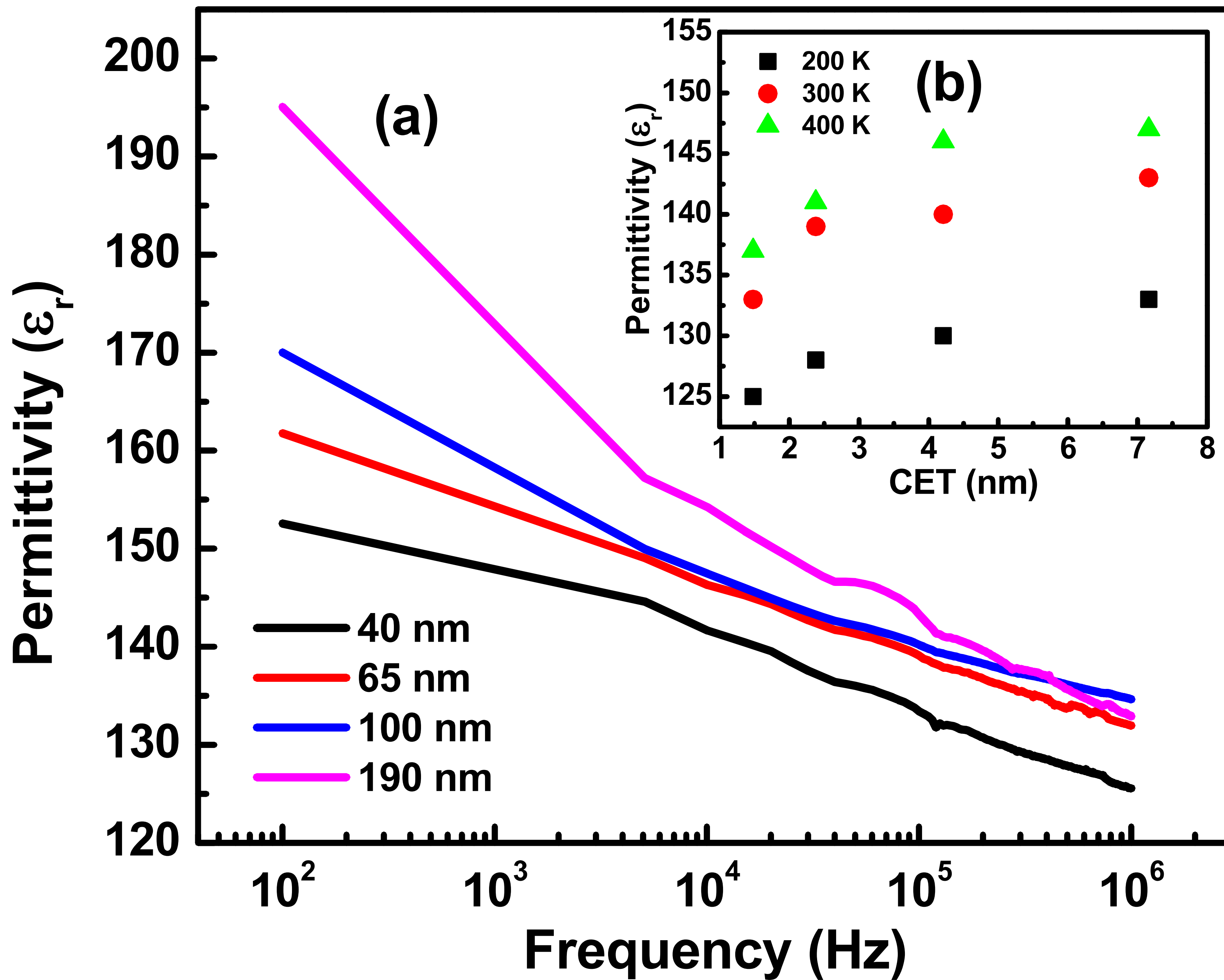
FIG. 4. Leakage current density of the dielectric stack with CET value 2.4 nm measured at four different temperatures. a) Room-temperature Schottky plot for the stack with CET value of 2.4 nm. b) Leakage current values of the four stacks vs capacitance density measured at 300 K and at 1 V.



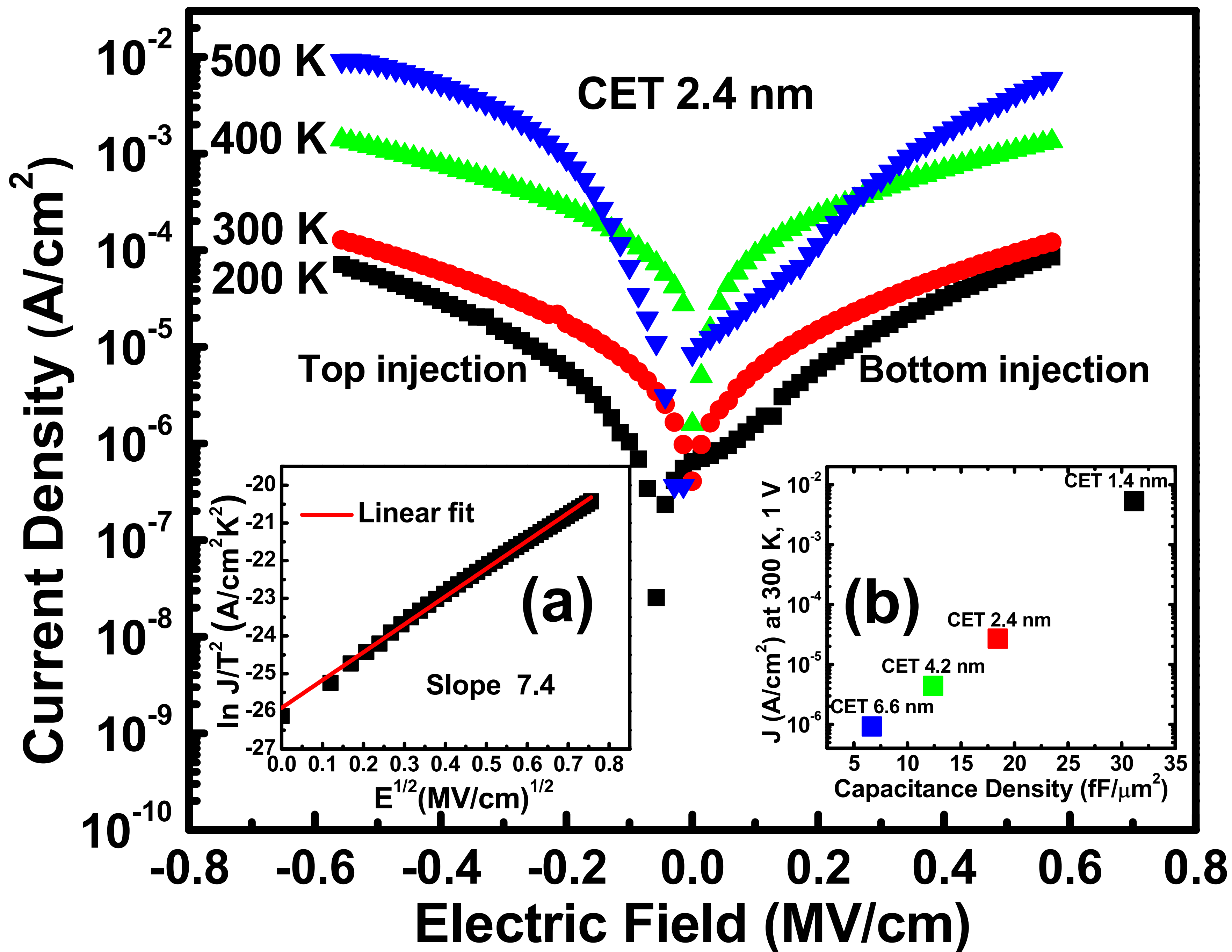
Capacitance Density (fF/μm²)
CET (nm)
200 K
300 K
400 K
@ 100 kHz
(a)
@ 100 kHz
Linear fit
CET=1.4 nm
Capacitance Density (fF/μm²)
T (K)
(b)
CET 1.4 nm
CET 2.4 nm
CET 4.2 nm
CET 6.6 nm
Capacitance Density (fF/μm²) @ 300 K
Frequency (Hz)



500
400
300
200
100
0
1
2
3
4
5
6
7
α (ppm/V²) @ 100 kHz
CET (nm)
200K
300K
400K
0.012
0.009
0.006
0.003
0.000
ΔC/C0
200 K
300 K
400 K
Voltage linearity fit
CET 1.4 nm
(a)
-1.5 -1.0 -0.5 0.0 0.5 1.0 1.5
Electric Field (MV/cm)
700
600
500
400
300
200
100
0
α (ppm/V²) @ 300K
(b)
CET 1.4 nm
CET 2.4 nm
CET 4.2 nm
CET 6.6 nm
10⁴ 10⁵ 10⁶
Frequency, Hz



(a)
(b)
Permittivity (ε_r)
Frequency (Hz)
40 nm
65 nm
100 nm
190 nm
200 K
300 K
400 K
CET (nm)



Current Density (A/cm2)
Electric Field (MV/cm)
CET 2.4 nm
500 K
400 K
300 K
200 K
Top injection
Bottom injection
Linear fit
(a)
Slope 7.4
ln J/T2 (A/cm2K2)
E1/2(MV/cm)1/2
(b)
CET 1.4 nm
CET 2.4 nm
CET 4.2 nm
CET 6.6 nm
J (A/cm2) at 300 K, 1 V
Capacitance Density (fF/μm2)