An electro-photo-sensitive memristor for neuromorphic and arithmetic computing

P. Maier,1 F. Hartmann,1 M. Emmerling,1 C. Schneider,1 M. Kamp,1 S. Höfling,1,2 and L. Worschech1

1 Technische Physik and Wilhelm Conrad Röntgen Research Center for Complex Material Systems, Physikalisches Institut, Universität Würzburg, Am Hubland, D-97074 Würzburg, Germany
2 SUPA, School of Physics and Astronomy, University of St. Andrews, St Andrews, KY16 9SS, United Kingdom

(Dated: July 11, 2016)

We present optically and electrically tunable conductance modifications of a site-controlled quantum dot memristor. The conductance of the device is tuned by electron localization on a quantum dot. The control of the conductance with voltage and low power light pulses enables applications in neuromorphic and arithmetic computing. As in neural networks, applying pre- and post-synaptic voltage pulses to the memristor allows to increase (potentiation) or decrease (depression) the conductance by tuning the time difference between the electrical pulses. Exploiting state-dependent thresholds for potentiation and depression, we were able to demonstrate a memory-dependent induction of learning. The discharging of the quantum dot can further be induced by low power light pulses in the nW-range. In combination with the state-dependent threshold voltage for discharging, this enables applications as generic building blocks to perform arithmetic operations in bases ranging from binary to decimal with low power optical excitation. Our findings allow the realization of optoelectronic memristor-based synapses in artificial neural networks with a memory-dependent induction of learning and enhanced functionality by performing arithmetic operations.

PACS numbers: 73.23.-b, 73.40.Gk, 84.35.+i, 87.19.lv

I. INTRODUCTION

In the human brain the interconnection of neurons via synapses results in a massively parallel computational network [1]. Synapses, the connections between neurons, are constantly formed or eliminated [2, 3] and learning is associated with the modification of their strength that regulates the transmission of action potentials [4]. This modification is controlled by the superposition of action potentials generated by pre- and post-synaptic neurons. According to the model of spike-timing-dependent plasticity (STDP), the relative timing of pre- and post-synaptic spikes is crucial for dynamic potentiation or depression [5–8]. In neural networks, neuronal activities do not necessarily result in changes of synaptic strength, but also in a varying capability for the induction of potentiation or depression [9, 10], which ensures intrinsic convergence of synaptic strength [11]. Recently, STDP was demonstrated with memristors [12–15] and interconnecting memristors with neurons, STDP-based learning rules can be emulated in self-learning visual cortices [16].

The memory resistance (memristance) of memristors can be controlled and altered by electrical and low power optical pulses. Applying nature-inspired voltage pulses to emulate the action potentials of pre- and post-synaptic neurons, the conductance of the device is raised (potentiation) or lowered (depression) by changing the time difference between the onsets of the pulses. We

Here we present an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic computing. The conductance of the device emerges from different amounts of quantum dot (QD) localized charges which can be controlled and altered by electrical and low power optical pulses. Applying nature-inspired voltage pulses to emulate the action potentials of pre- and post-synaptic neurons, the conductance of the device is raised (potentiation) or lowered (depression) by changing the time difference between the onsets of the pulses. We
further observe a dependence of the conductance change on the initial state, which was set by the past biasing procedure. Thus previous input pulses are memorized and the capability for the induction of learning changes accordingly. Finally, we demonstrate an optical control of the memristor. Combining the optical tunability with the state-dependent threshold for potentiation, the device is a basic component for the realization of arithmetic operations with low power optical pulses.

II. DEVICE LAYOUT

Fig. 1(a) shows a scheme of the device, which is based on a GaAs/AlGaAs heterostructure with precisely positioned InAs QDs (highlighted in green). The fabrication process is described in detail in Ref. [32]. The memristive operation is realized by short-circuiting the source with the gate contacts (see Fig. 1(b)) [20, 21]. This wiring scheme is known as diode connected transistor and can for example be used as temperature sensor [33]. In our case the transistor is a quantum dot floating gate transistor. In analogy to synapses in neural networks, where the plasticity is controlled by the action potentials of pre-and post-synaptic neurons, we apply two independent voltage pulses labelled as pre- and post-synaptic pulses to the two terminals of the device. The voltages $V_{pr}$ and $V_{po}$ are applied to the source and drain contacts, respectively (see Fig. 1(b)). The current $I$ was measured as voltage drop across a resistor with $R = 1$ MΩ in series to the channel. All measurements were conducted at 4.2 K.

III. MEMRISTOR CHARACTERISTICS

Fig. 1(c) depicts the current-voltage-characteristic of the device. A closed voltage sweep of the voltage applied to the source and gate contacts between $-3.8$ and $4.6$ V shows a pinched hysteresis loop, the fingerprint of memristors [34]. The low and high conductance values between $-1$ and $1$ V are explained by different amounts of QD-localized electrons $n$ with more charges corresponding to the smaller conductance. $V_{th}$ is the width of the plateau with almost zero conductance and is linear dependent on the amount of localized electrons [21]. The QD becomes charged for voltages below $V_C \approx -1.9$ V ($\Delta n > 0$) and discharged above $V_d \approx 4.4$ V ($\Delta n < 0$). In Fig. 1(c), $V_C$ and $V_d$ are highlighted with the red vertical lines. Hence the conductance of the device is altered by changing the amount of QD-localized charges which depends sensitively on the time and the voltage value spent above the discharging or below the charging voltage.

The pinched hysteresis loop can be analysed by the width $V_{th}$ of the plateau with almost zero conductance [21]. Fig. 1(d) displays the discharging voltage in dependence on $V_{th}$. $V_{th}$ was increased by reducing the minimum bias voltage during the voltage sweep cycle in Fig. 1(c). Lower minimum voltages lead to more localized electrons and enhanced $V_{th}$ [21]. A linear increase of $V_d$ is observed for raising $V_{th}$. Strukov et al. explained the dependency of the threshold voltage on the state of the memristor with non-linearities in ion movements [32]. Here we describe the shift of the discharging voltage by means of a charge-dependent gate efficiency. Charging the QD with electrons lowers the gate-channel-capacitance. The quantum dot charge dependent gate-channel-capacitance emerges from the depletion of the channel via localized electrons on the quantum dot which effectively leads to a variable effective gate-channel distance with different charge accumulation interfaces. Thus discharging the QD leads to larger capacitances. Controlling the amount of localized charge with the lateral gates, a hysteresis in the capacitance-voltage-curve is evident, which is the fingerprint of memcapacitors [10, 36]. For reduced capacitances, larger absolute gate voltages are required to shift the potentials of the QD and the two-dimensional electron gas by the same energy. Thus the charging and discharging voltages are reduced and increased, respectively.

For excitation with constant parameters (voltage range, sweep time), the pinched hysteresis loop as well as the threshold voltages $V_d$ and $V_C$ are highly reliable

FIG. 1. (a) Scheme of the memristor. The positions of the QDs are highlighted in green. (b) Circuit diagram of the memristor. $V_{pr}$ is applied to the top contact of the wire and the lateral gates. $V_{po}$ is applied to the bottom contact of the wire. (c) Current-voltage-characteristic of the device. $V_C$ and $V_d$ are the threshold voltages for charging and discharging, respectively. (d) Linear dependency between the discharging voltage and $V_{th}$. 

V
IV. SPIKE-TIMING-DEPENDENT PLASTICITY

Two function generators were used to emulate the voltage pulses in Fig. 2(a), that were applied to the two terminals of the device (see Fig. 4(b)). The general shape of the pulses was chosen to mimic an action potential measured in the axon of a squid [37]. Simple rectangular pulses are not used, because they only enable to either emulate potentiation or depression with a single set of pulses [21]. However, the transition from potentiation to depression solely triggered by the timing of the pulses is essential to mimic STDP and requires pulse shapes with positive and negative amplitudes. These pulse shapes allow to change the voltage difference across the memristor from negative to positive by inverting the temporal order of the two pulses. Thus charging or discharging of the QD can be induced depending on the order of the pulses. Because of the asymmetric charging and discharging voltages of the device, at least one pulse needs to be asymmetric. Thus we used amplitudes of (+4.2, −3.1) and (+2.0, −2.0) V for $V_{po}$ and $V_{pr}$, respectively. The pulse widths were 10 ms. The time difference $\Delta t$ between the pulses is the crucial parameter of STDP. Here, the post-synaptic pulse is applied after the pre-synaptic pulse for positive time differences and vice versa.

For the present device, the performance is mainly governed by the voltage difference $V_{pr} - V_{po}$ between the two terminals. Depending on $\Delta t$, the temporal voltage difference can exceed the threshold voltages for charging and discharging (see red highlighted areas in Fig. 2(b)) for their respective times $T_c$ and $T_d$. These time intervals depend on $\Delta t$, i.e., $T_c(\Delta t)$ and $T_d(\Delta t)$, as sketched in Fig. 2(c). For simple rectangular pulses, either $T_c$ or $T_d$ would be zero and independent on $\Delta t$. Thus tuning the time difference does not allow the observation of a transition from depression to potentiation. For the pulses in Fig. 2(a), the dominant processes are charging (highlighted in yellow) for negative and discharging (highlighted in green) for positive time differences. The time dependent tunneling from the two-dimensional electron gas to the QD (charging) and from the QD to the two-dimensional electron gas (discharging) can be described by a capacitor model [38]. The dependency of $n$ on $T_c$ and $T_d$ is given by

$$n(\Delta t) = n_0 + n_+ \frac{1 - \exp \left( \frac{-T_c(\Delta t)}{\tau_c} \right)}{1 - \exp \left( \frac{-T_d(\Delta t)}{\tau_d} \right)} - n_- \frac{1 - \exp \left( \frac{-T_d(\Delta t)}{\tau_d} \right)}{1 - \exp \left( \frac{-T_c(\Delta t)}{\tau_c} \right)},$$

where $n_0$ is the initial amount of QD-localized charges. The second and third term of equation (1) represent charging and discharging characteristics with time constants $\tau_c$ and $\tau_d$, respectively. $n_+$ and $n_-$ are constants that represent the total amount of transferred charges.

Fig. 3(a) shows the conductance of the memristor versus the number of applied pulses $N$ for different $\Delta t$. Here, one pulse is defined as pair of the pulses depicted in Fig. 2(a). Ten consecutive pulses were applied for constant time differences. Each pulse is followed by a read-out pulse with amplitude 2.8 V and width 5 ms to determine the conductance $G$. For large time differences ($\pm 5.3$ ms), the conductance remains almost unaltered up to ten pulses. Smaller time differences lead to an increase and decrease of the conductance with $N$ for +0.7 and −0.7 ms, respectively. These observations are due to changes in the voltage difference across the memristor as a function of $\Delta t$. Varying time differences lead to different time intervals $T_c(\Delta t)$ and $T_d(\Delta t)$. For $\Delta t = \pm 5.3$ ms, they are almost zero and thus $T_d/T_c \approx 0$ and $T_c/\tau_c \approx 0$. Consequently the amount of QD-localized charges in equation (1) remains unaltered with $n(\Delta t) \approx n_0$ and
\[ G_N = \frac{G_0(1 - \exp(-N/T_c)}{1 + \exp(-N/T_c)} \]
(+4.2, −2.8) V for $V_{pr}$ and (+2.0, −2.0) V for $V_{po}$. Again, the conductance increases and decreases for positive and negative time differences, respectively. Consequently, the conductance change after one pulse $G_1 - G_0$ versus $G_0$ is positive (potentiation) for $\Delta t = +0.9$ ms and negative (depression) for $\Delta t = −1.1$ ms (see Fig. 4(c)). While $G_1 - G_0$ decreases linearly for depression, it shows a non-linear response with a maximum at 1 µS for potentiation. The initial conductance corresponds to an initial amount of QD-localized charges $n_0$ and thus controls the threshold voltages for charging and discharging (as shown in Fig. 4(d) for $V_d$). For decreasing $n_0$ (corresponds to increasing $G_0$), the discharging voltage is lowered and the charging voltage is raised linearly because both are proportional to $n_0 e/C$. Thus larger initial conductance values enhance the times $T_d$ and $T_c$ for constant bias voltages which in turn lead to larger absolute values of $G_1 - G_0$ (see equation (3)). The proportionality between $V_c$ and $n_0$ is directly reflected in the linear $G_1 - G_0 (G_0)$ - curve for a time difference of −1.1 ms. For potentiation, the linear increase is superimposed by a decline, which originates from the saturation of the conductance at the maximum value (discharged QD). In equation (4), $n$, correspond to the number of electrons that tunnel out of the QD. This number is limited by $n$, i.e. $n \leq n$. For $G_0 > 1$ µS, the number of tunneling electrons equals $n$. Consequently, this number is reduced for increasing $G_0$ which according to equation (4) lowers the absolute conductance change.

Fig. 4(d) presents the relative conductance change after a single pulse versus the initial conductance. $\Delta G$ is almost constant and independent on the initial conductance value for depression, but ranges from 0 to 120 % for potentiation. Similar findings in hippocampal neurons showed relative changes of synaptic strength (absolute change divided by initial value) that depend on the initial strength for potentiation but are constant for depression, which is an important stability feature of STDP models [8, 11]. The reason therefore is that the synaptic strength triggers post-synaptic activity, and thus a constant relative change for potentiation would cause infinite synaptic strengths. A dependency of the relative change on the initial strength prevents this positive feedback and ensures converging synaptic strengths [11]. With the relative conductance change dependent on the initial conductance value, memristor-based synapses thus allow to prevent the positive feedback in artificial neural networks, where the pulses are generated intrinsically by post-synaptic activities, and ensure converging conductances.

Conductance traces versus $N$ for 200 consecutive pulse pairs are displayed in Fig. 5(a). In the following, pulse pairs of pre- and post-synaptic pulses with negative and positive time differences are labeled as depression and potentiation pulses, respectively. The data in Fig. 5(a) was measured by applying $N_d$ depression pulses with time difference of −1 ms, followed by $N_p$ potentiation pulses with time difference of +1 ms. The amplitude of $V_m$ was raised from 4.2 to 4.5 V to realize large positive conductance changes. The curves represent $N_d = N_p = 5, 10$ and 20 from top to bottom. Since the conductance can be decreased for negative and increased for positive time differences, it alternates periodically by inverting the temporal order of the pulses. The conductance value $G_d$ after $N_d$ depression pulses (before potentiation) shows an exponential decay versus $N_d$, as shown in Fig. 5(b). The dashed line represents the exponential fit function according to equation (8). The conductance reduction per pulse is lowered for larger $N_d$ and thus many pulses are necessary to reduce $G_d$ to zero. Information learned by previous potentiation is stored for a long time because of the intrinsic non-volatile memory functionality of memristors. The storage capability enables long-term storage (several days at 4.2 K for the present device) of conductance values even for zero bias, which is advantageous compared to simple RC circuits that also show exponential conductance reductions.

Conductance traces for different numbers of depression pulses with alternating time difference $G$ is depressed and potentiated depending on the sign of $\Delta t$. The curves represent $N_d = N_p = 5, 10$ and 20 from top to bottom. (b) Conductance $G_d$ after $N_d$ depression pulses versus $N_d$. $G_d$ decreases exponentially with increasing number of depression pulses. (c) Conductance traces for 400 consecutive pulse pairs with $N_p = 200 - N_d$. Applying $N_d$ depression pulses requires $\Delta N$ pulses to raise $G$ up to 50 % of the maximum value. $\Delta N$ versus $N_d$ shows an exponential dependency, as displayed in (d).

![Fig. 5](image-url)
and potentiation pulses \( N_p = 200 - N_d \) are presented in Fig. 5(c) for 400 consecutive pulse pairs. The number of potentiation pulses \( \Delta N \) to raise the conductance up to 50% of the maximum value increases for larger \( N_d \) (lower \( G_d \)). The exponential increase of \( \Delta N \) versus \( N_d \) in Fig. 5(d) can be explained bearing in mind that the application of more depression pulses leads to an enhanced amount of QD-localized charges. Thus the threshold voltage for discharging shifts towards larger values (see Fig. 5(d)) and the time interval \( T_d \) for the consecutive potentiation is lowered. According to equation (6), more pulses are needed to compensate the reduction of \( T_d \). This explains the exponential \( \Delta N - N_d \) dependence as shown in Fig. 5(d). A correlation between the thresholds for potentiation and depression on the initial synaptic strength (here \( G_0 \)) was also observed in the goldfish Mauthner cell [41]. Our findings of the \( \Delta N - N_d \) dependence enables the implementation of a memory-dependent induction of learning. Here, the number of depression pulses controls the strength before potentiation is induced by learning. The increase of \( \Delta N \) for large \( N_d \) (small initial strengths) implies that potentiation and thus learning is more effective for larger initial strengths, which corresponds to the memory of previous learning processes.

VI. OPTICAL CONDUCTANCE-CONTROL

So far, the presented results may be reproducible with Si-based floating gate transistors with advantages of reduced dimensionality, room temperature operation and CMOS compatibility [24]. The presented device is based on a GaAs/AlGaAs heterostructure and it is thus fully compatible with other III-V based and state-of the art optoelectronic semiconductor devices. Due to its direct band gap, the material offers better absorption coefficients compared to similar silicon based device realizations and hence allow to control the memristance by electrical and low power optical pulses as shown in Figs. 4 and 7. For the optical excitation, a red light emitting diode (LED) with wavelength \( \lambda = 632 \text{ nm} \) was placed beside the device and illuminates the whole sample. For optical excitation, the red LED was placed beside the device and illuminates the whole sample. (b) Current-voltage-characteristics under cw-illumination with light powers below 1 nW. The vertical red lines indicate the charging and discharging voltages for a LED current of 0.035 \( \mu \text{A} \).

VII. ARITHMETIC COMPUTING

The device with its optical control of the QD localized charge and state-dependent threshold voltage for discharging is a basic component to perform arithmetic operations with optical pulses. Fig. 4(b) displays the conductance versus pulse number for optical and electrical excitation. We excited the memristor with 10 consecutive light pulses with a light power of 1 nW and a width of 10 \( \mu \text{s} \) after 2000 pulses. For decreasing light power, more pulses are required to raise the conductance above zero. The conductance remains unaltered for 2000 pulses with a power of 3 nW and below. Because the amount of transferred electrons is controlled by the width and the power of the light pulses, i.e. the number of incoming photons, larger excitation powers enables discharging with shorter light pulses. In Ref. [13], photo-induced charging of the QD in a similar structure was demonstrated with light in the telecommunication range. Thus we believe that the presented device allows bi-directional, light-induced conductance changes.
mined the conductance of the memristor by applying a read-out pulse with amplitude 1.3 V. Before the measurement \((N = 0 \text{ in Fig. 7(b)})\), the QD was charged by an initializing pulse with an amplitude of \(-3.8 \text{ V}\) and thus the conductance is small. Applying only electrical pulses (switched off LED), the conductance remains almost unaltered up to ten pulses. Because the discharging voltage is larger than the amplitude of 4.46 V, the QD is not completely discharged and the conductance is not affected. For electrical and optical excitation, the conductance is raised successively. Each light pulse partially discharges the QD and thus enhances the conductance and reduces the discharging voltage (see Fig. 7(d)). After the 9th pulse, the discharging voltage is smaller than the electrical pulse amplitude of 4.46 V and the QD becomes fully discharged. A steep increase of the conductance occurs, as shown in Fig. 7(b). With the well pronounced conductance enhancement after the 9th pulse, the memristor is suitable for basic arithmetic operations as counting or adding in base 10. From 1 to 9 pulses, the conductance increases from 0.09 \(\mu\text{S}\) to 1.16 \(\mu\text{S}\) and for the tenth pulse a sudden raise of the conductance to 2.2 \(\mu\text{S}\) is observed. An addition can be performed by applying specific numbers of optical pulses that represent the addends. Multi-digit operations are required if the sum of the addition exceeds the base and can be realized by combining several memristors and reset circuits to a network [44]. The reset circuits set the state variable to the initial value (reset to zero) and additionally provide the carry signal for the next significant bit. After the operation, the conductance corresponds to a certain pulse number, which is the result of the addition. In analogy to the implementations in Ref. [45], subtraction, multiplication and division can be performed. The large conductance enhancement after the tenth pulse is only possible because of the state-dependent threshold voltage for discharging and allows to trigger the reset with high accuracy and low impact of undesirable readout noise. For practical applications, this well-defined conductance state for a discharged QD triggers the release of an initialization pulse, which can be employed by additional circuitry (on-chip fabrication of comparator). In analogy to synapses in neural networks, the memristor combines processing of information and memory. The result of the arithmetic operation is stored as conductance of the memristor. Similar results have been reported for phase change materials with much larger excitation powers [46]. Here, the direct band gap leads to high absorption coefficients and the device structure with a single QD controlling the memristance allows to tune the conductance state by absorbing only a low number of photons. The optical control of the QD charge thus employs an efficient and low power possibility for arithmetic operations of light pulses.

Fig. 8(a) depicts the conductance versus number of optical pulses with different light powers. An addition can be performed by applying specific numbers of optical pulses that represent the addends. Multi-digit operations are required if the sum of the addition exceeds the base and can be realized by combining several memristors and reset circuits to a network [44]. The reset circuits set the state variable to the initial value (reset to zero) and additionally provide the carry signal for the next significant bit. After the operation, the conductance corresponds to a certain pulse number, which is the result of the addition. In analogy to the implementations in Ref. [45], subtraction, multiplication and division can be performed. The large conductance enhancement after the tenth pulse is only possible because of the state-dependent threshold voltage for discharging and allows to trigger the reset with high accuracy and low impact of undesirable readout noise. For practical applications, this well-defined conductance state for a discharged QD triggers the release of an initialization pulse, which can be employed by additional circuitry (on-chip fabrication of comparator). In analogy to synapses in neural networks, the memristor combines processing of information and memory. The result of the arithmetic operation is stored as conductance of the memristor. Similar results have been reported for phase change materials with much larger excitation powers [46]. Here, the direct band gap leads to high absorption coefficients and the device structure with a single QD controlling the memristance allows to tune the conductance state by absorbing only a low number of photons. The optical control of the QD charge thus employs an efficient and low power possibility for arithmetic operations of light pulses.

FIG. 7. (a) Conductance versus number of optical pulses with different light powers. (b) Conductance traces for 10 consecutive electrical pulses (LED: off) and pulse pairs of electrical and optical pulses (LED: on). (c) Schematic time trace of the applied electrical (blue) and optical (green) pulses.

VIII. CONCLUSION

In summary, we presented an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic
computing. Similar to synaptic strength in neural networks, the conductance is controlled by the time difference of incoming voltage pulses. In addition, the threshold voltages to switch the conductance of the device were shown to be state-dependent, which emerges from the interplay of a memristance with a memcapacitance. In contrast to other realizations of memristors, \[^{47,49}\] memristance and memcapacitance switching of the presented device are observed between different terminals. The memristance is measured in the two-terminal geometry and the memcapacitance between the lateral gates and the wire. Thus the state of the device controls the charging and discharging voltages via the gate-channel-capacitance (intrinsic feedback). This may enable the implementation of memory-dependent induction of learning or the realization of counters and integrate-and-fire neurons. Here we exploited the feedback to show the capability of performing arithmetic operations in different bases with clearly distinguishable reset states.

The large pulse widths of several ms and low operation temperature prevent immediate application of the presented device in artificial neural networks. The maximum operation temperature of the device may be enhanced to room temperature by tuning the material composition of the quantum dots and the surrounding matrix.\[^{31,50}\] The widths of the pulses can be reduced by increasing the amplitude and power of the electrical and optical pulses, respectively. Write times of 6 ns have been already reported for InAs quantum dots in a GaAs matrix.\[^{51}\] The presented results demonstrate the capability of emulating synaptic functionalities in combination with performing basic arithmetic operations in different bases and may trigger future research regarding the material composition to enhance the maximum operation temperature. With operation at room temperature, the device may be employed in memristor-based non-von Neumann architectures to implement brain-inspired computing with a memory-dependent induction of learning.

**ACKNOWLEDGEMENTS**

The authors gratefully acknowledge financial support from the European Union (FPVII (2007-2013) under grant agreement n 318287 Landauer) as well as the state of Bavaria.

---


