Development of Control Circuitry for Charge Coupled Devices

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Declaration for the Degree of M.Sc.

I, James McGregor Wade hereby certify that this thesis has been composed by myself, that it is a record of my own work, and that it has not been accepted in partial or complete fulfilment of any other degree or professional qualification.

Signed: Date: 24/09/90

Abstract

A study of Charge Coupled Devices (CCD) was carried out. Various CCD drive methods were investigated to support a CCD imaging sensor. The development of drive circuitry to support imaging CCD's. Also developed was circuitry to convert the analogue waveform from the CCD sensor into digital information that was subsequently stored. Laboratory instruments constructed from the above circuitry. Various applications for laser research of CCD's was demonstrated.

Acknowledgements

I would like to thank my supervisor Dr James L. Lawrence for all his encouragement, help and support, which he gave so freely both during the research and in the writing of this thesis.

I would like to thank Professor Wilson Sibbett and the University of St Andrews for giving me the opportunity to undertake a Master of Science degree.

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CHAPTER 1

INTRODUCTION

1. CHARGE-COUPLED DEVICES

Charge-coupled devices were developed in the late 1960's and since then they have been used in a variety of applications, as memory devices, in signal processing and in imaging. In this thesis, a variety of applications of the use of CCD's to the capture and analysis of laser events will be described.

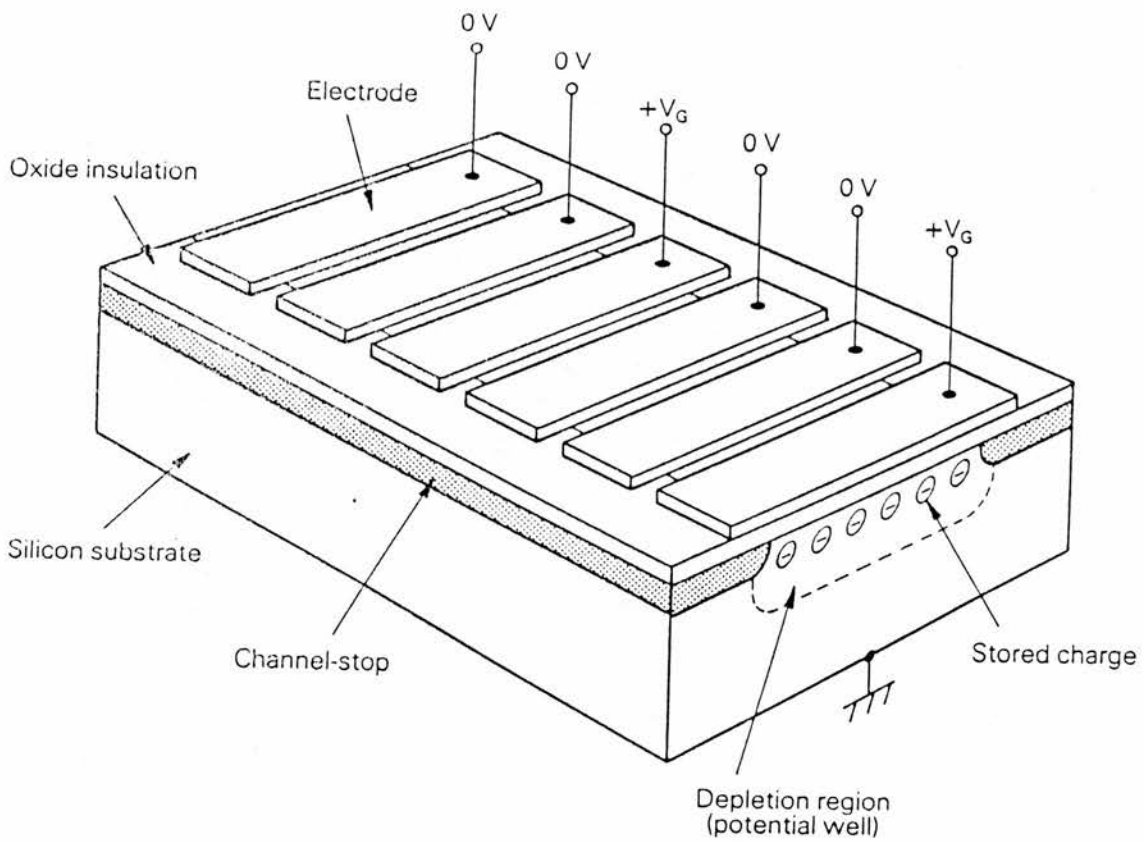


Figure 1.1. Basic CCD Structure

CHAPTER 1. INTRODUCTION

In its simplest form, a charge-coupled device is an array of closely spaced MOS capacitors. The fundamental unit consists of three metal electrodes on the surface of a thin layer of silicon oxide which is itself situated on either n- or p-type silicon. On each side of the storage region is placed a channel stop to prevent the charge from dispersing. The channel stop is constructed from reverse doped silicon from that of the substrate. The whole device consists of many such units arranged in either a linear or a two-dimensional array and if a charge packet is place under one of the electrodes, this packet can be moved at high speed along the line of electrodes. An example is shown in figure 1.1 with an n-type silicon substrate. Here two units are shown and the charge packet consists of electrons. The electrodes above the packet are at a positive potential and the other two electrodes in each unit are at zero potential.

To move a charge packet from beneath one electrode to its neighbouring electrode on the right hand side (figure 1.2(a)) that electrode is firstly raised to a high potential (figure 1.2(b)) and the charge packet will be distributed beneath both electrodes. The potential of the first electrode is then reduced to zero, pushing the remaining charge out to the right-hand side electrode (figure 1.2(c)). Thus these changes in potential have had the effect of dragging the charge packet from under one electrode to under its neighbouring electrode. To move charge packets over many units, three-phase clock signals of the form shown in figure 1.3 have to be applied. This clock is in common to each unit and only one clock generator is required for the whole

array. If this three-phase signal is applied to the electrodes of figure 1.4 then all the charge packets on that array will be moved simultaneously.

When the charge packet reaches the end of the array it is captured by a charge detection amplifier which converts the charge packet into a proportional analogue voltage which then enables the signal to be monitored externally.

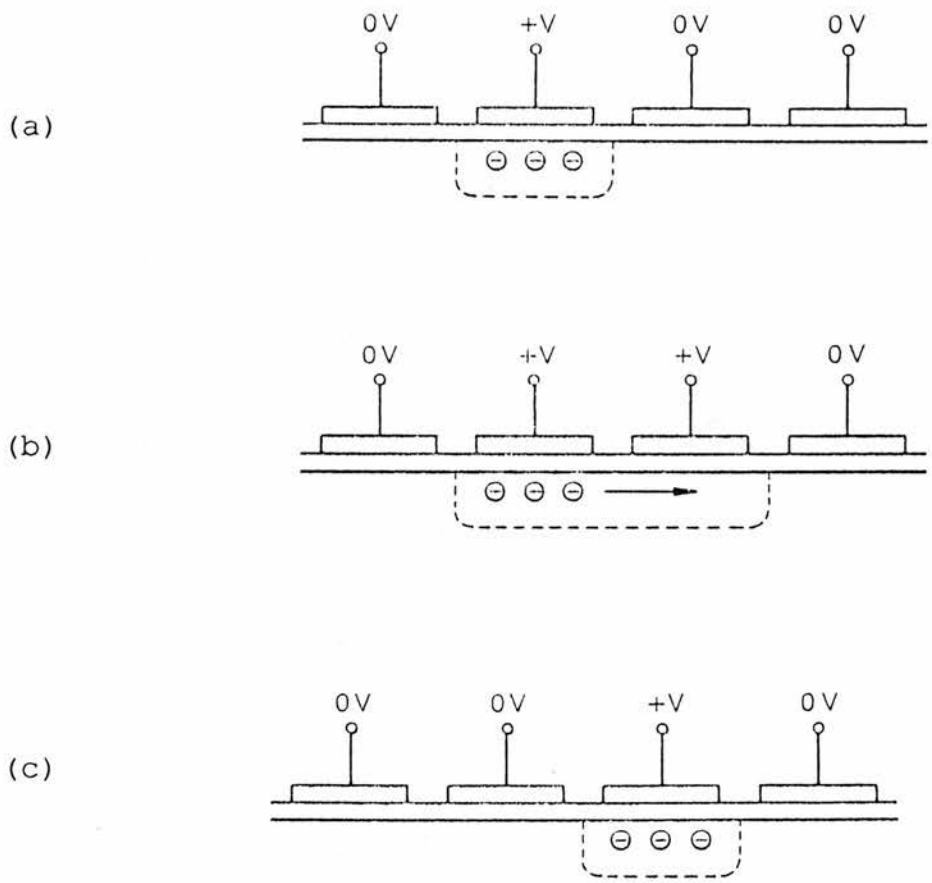


Figure 1.2. Charge Transfer.

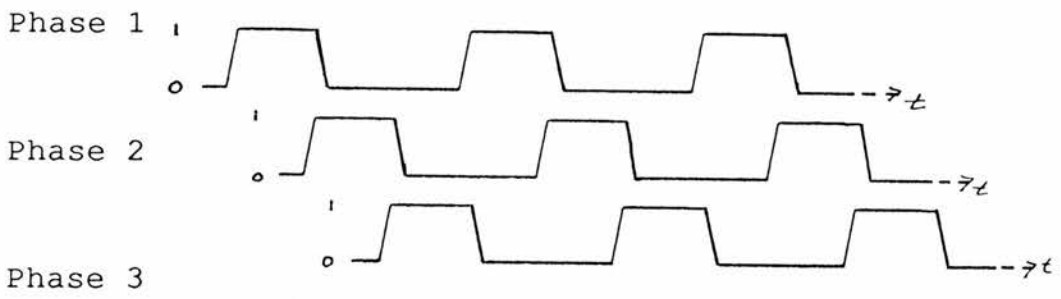


Figure 1.3. Three-Phase Clock.

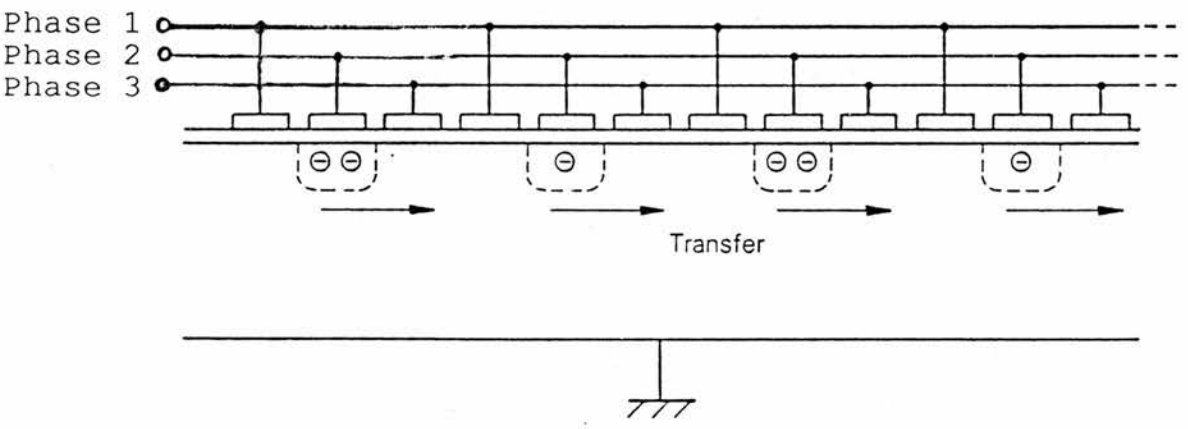


Figure 1.4. Simultaneous Charge Transfers.

These devices can be used as memory devices. As such, the existence of a charged packet is logic 1 while the absence of a charged packet is logic 0 and detector circuitry can be included to detect the binary digits. In imaging, a photon

of light incident on to the substrate will produce an electron-hole pair and this electron will be captured under the high potential electrode. Thus the total charge under the electrode will be proportional to the light intensity on that area and in this way a "picture" of an event can be captured.

The two main problems that arise with CCD imaging devices are saturation and dark current. If the incident light is too intense or if the time for which the light illuminates is too great, the number of electrons will reach the maximum which can be held under an electrode. Saturation of that area of the CCD will occur and it will contain no information. Dark current arises from the thermal generation of electrons which will accumulate in the CCD during exposure time and will add to the signal being detected. This dark current is very temperature dependent. It limits the exposure time and necessitates the removal of the accumulated signal at very high speeds and, in some applications, e.g. astronomy, the CCD's have to be cooled to fairly low temperatures to permit long exposures.

A linear CCD consists of a single line of elements and is shown schematically in figure 1.5.

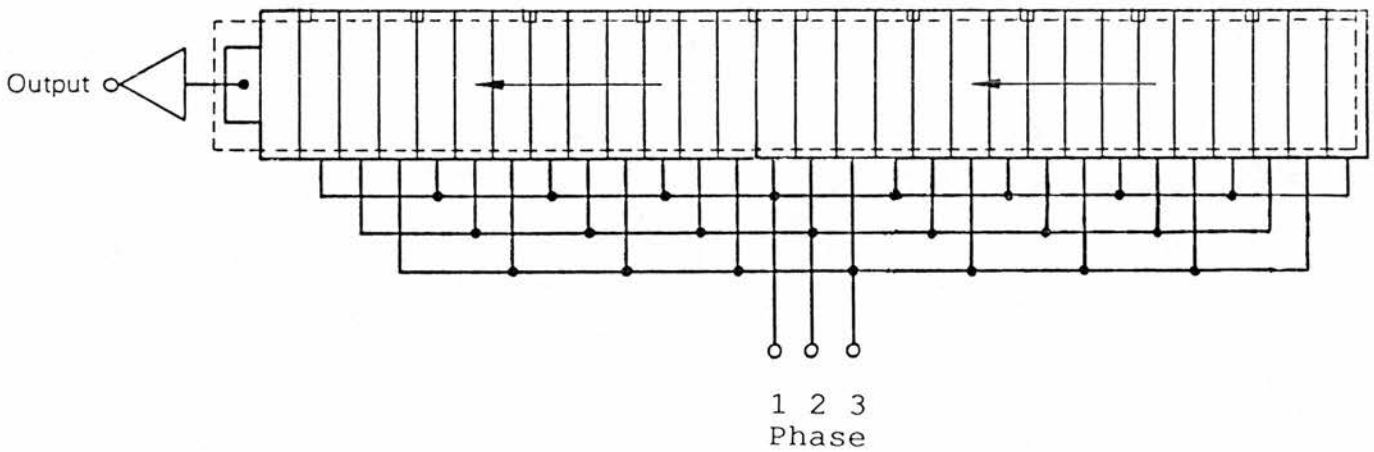


Figure 1.5. Linear CCD Array.

A schematic drawing of a two-dimensional CCD is shown in figure 1.6. The device consists of two main sections, The imaging section is where the light photons are allowed to produce the charge packets. The charges can then be quickly moved down into an equal area, the store section, which is shielded from the light. From there, the longer process of reading out the information serially can be achieved by pulsing one element from each column into the readout section then pulsing out that line. It is also possible to digitize the packet for transmission to a computer system.

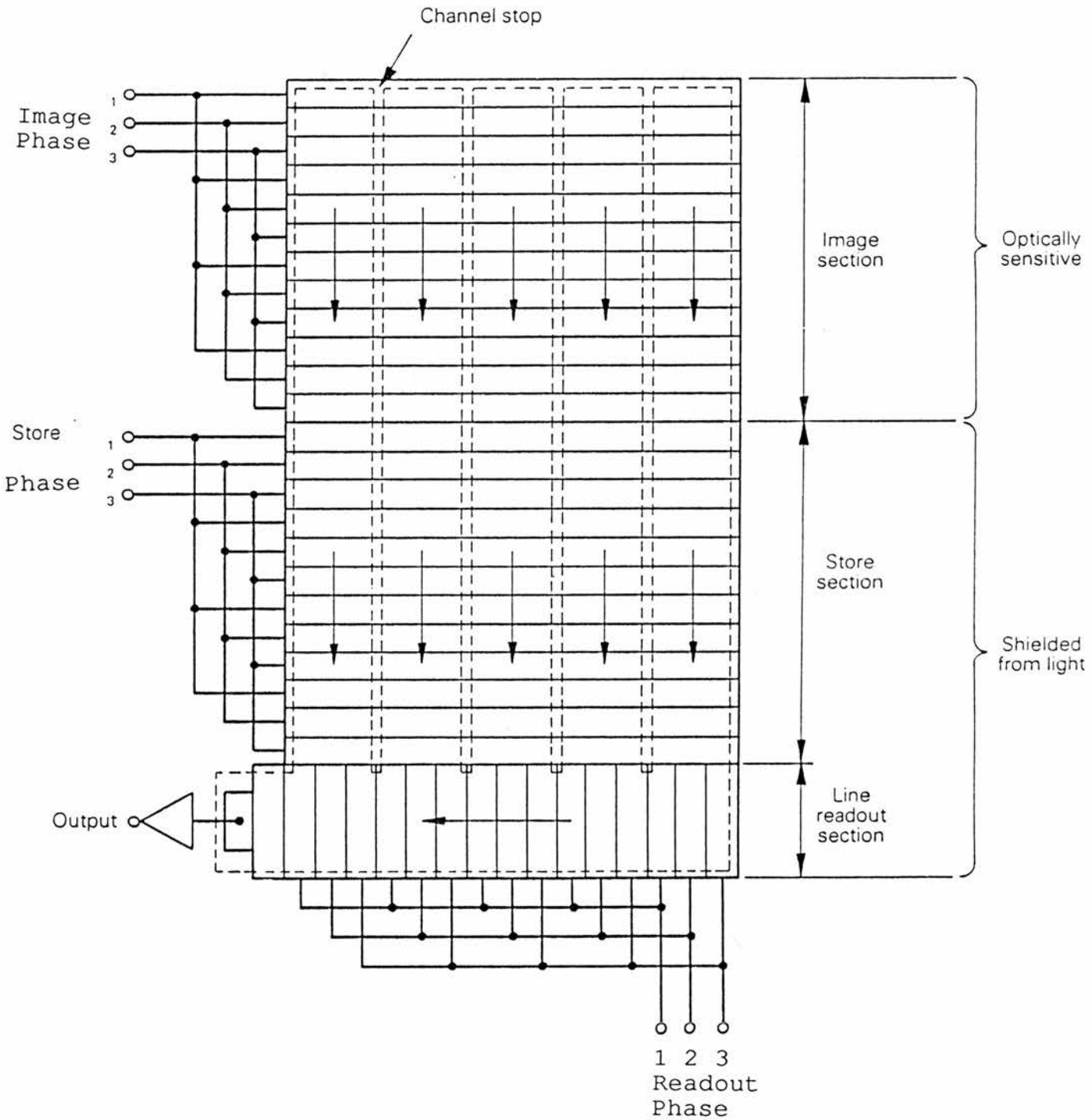


Figure 1.6. Two-Dimension CCD Array.

CHAPTER 2

512 BIT CCD CAMERA AND DIGITIZER

Chapter 2. 512 Bit CCD Camera and Digitizer.

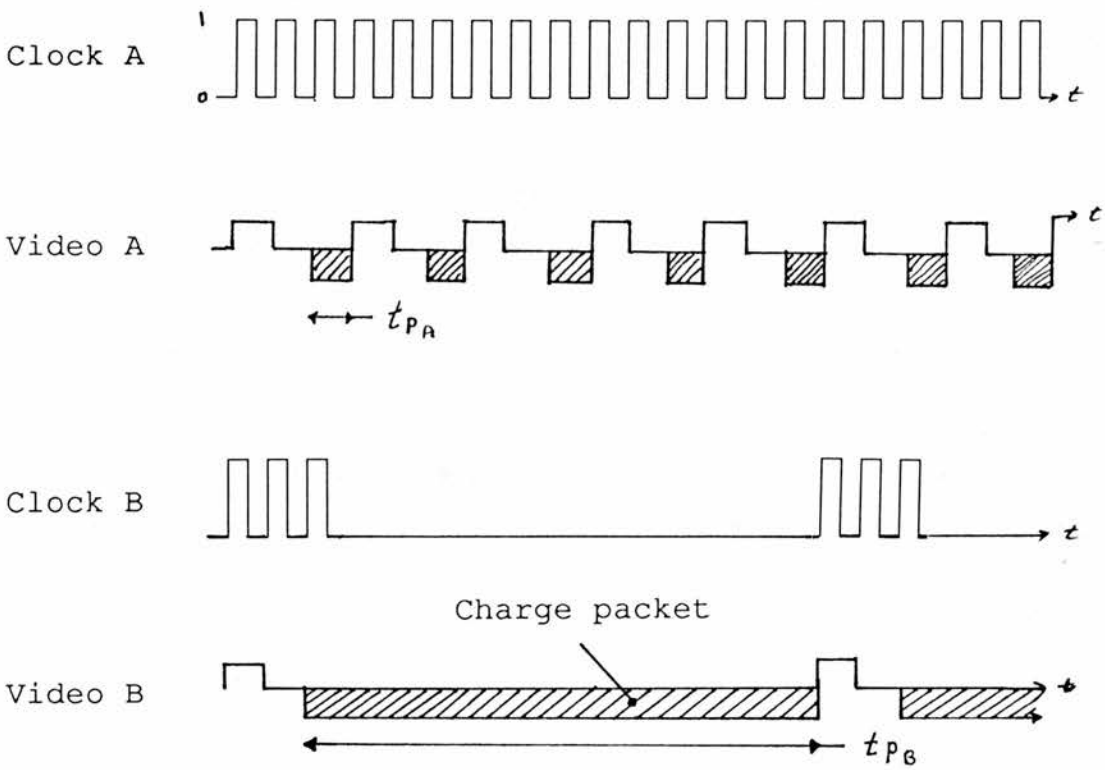
1.1. INTRODUCTION

The 512 bit linear CCD camera and digitizer was developed as a laboratory instrument for laser research and has been in use for over three years. The complete instrument allows single dimension optical sensing of an image and incorporates variable integration time (aperture exposure time) for its 512 photo-sensors. Event critical applications can be synchronised to the laser by means of an external trigger input allowing flexibility in use. Data can be directly monitored with the use of an oscilloscope, stored permanently on its internal 16 channel store or printed out on a X/t recorder.

IMEC, the manufacturers of the CCD have recommended that the drive circuit uses a shift register to generate the three phase drive waveforms. The video output charge packet would then be present in a one in three ratio. This has the advantage of using simple drive electronics, but requires longer readout times for a complete line of video to be read out. This instrument incorporates a compressed charge transfer and stretched readout timing generator that enables the video output charge packet to be present over a ratio of eleven in twelve as shown in figure 2.1.1. This timing yields faster readout times and leads to reduced dark current build-up. As a direct result the operator may now directly monitor the head output in high clarity.

This chapter deals with the design of the complete instrument and starts with a discussion of the CCD and follows with a block schematic diagram of the circuitry with a brief discussion of each block and its integrity with the

system. Each block is then discussed in detail down to component level. The instrument is then shown as a working laboratory instrument with some plotter graphs of actual application data.



Clock A with a 50% duty cycle.

Clock B with stretched and compressed duty cycle.
$t_{P_A} = t_{P_B}$

Figure 2.1.1 Comparison between video hold time.

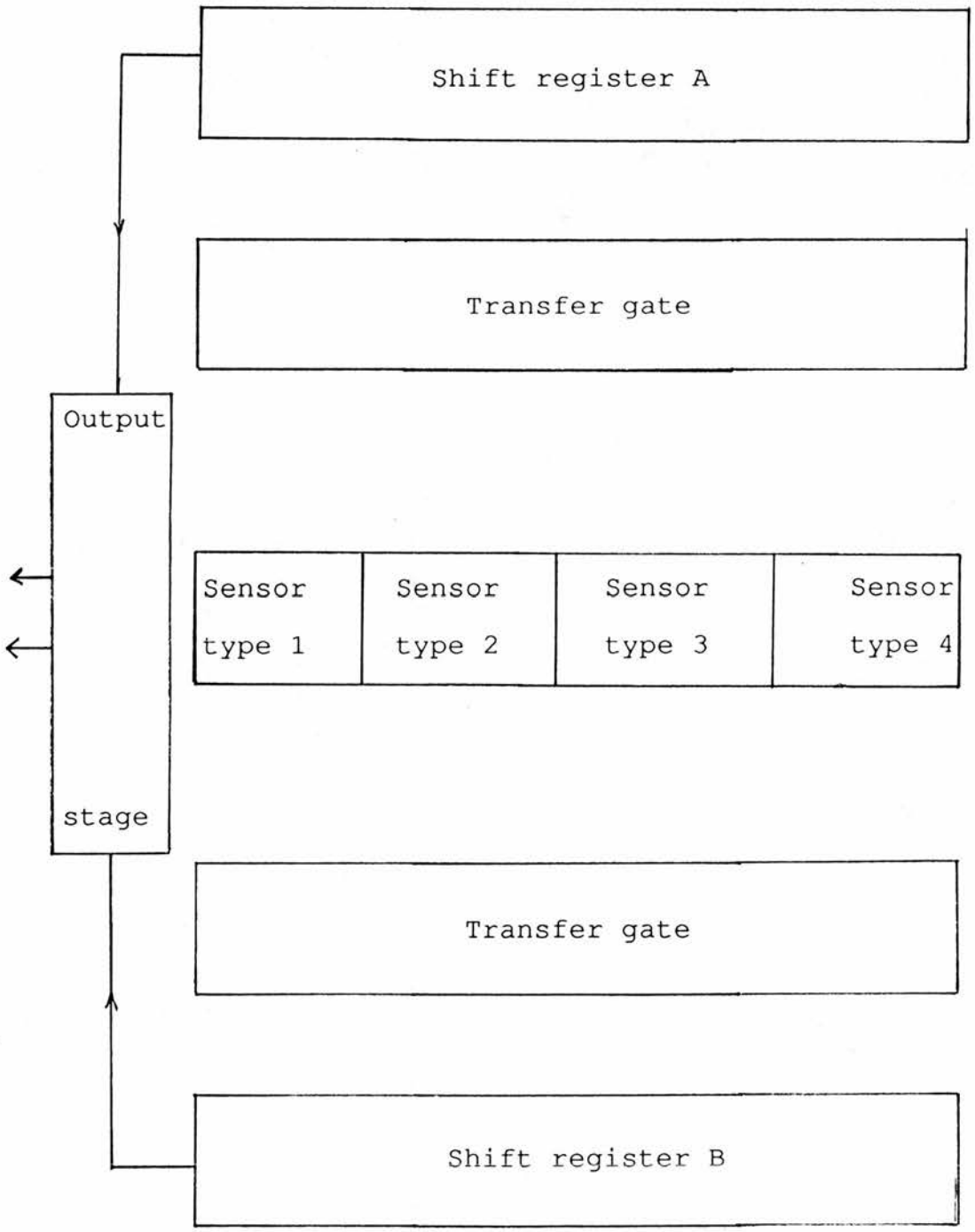


Figure 2.2.1. Block schematic of IMEC test CCD.

2.2. IMEC ESA512 DESCRIPTION

The Interuniversitair Micro-Electronic Centrum ESA-512 test CCD is a bilinear single dimension array using different technologies to construct four different sensor types as shown in figure 2.2.1. The CCD was designed and fabricated at the ESAT laboratories. The device consists of 512 photo sensors and two CCD readout registers with their outputs interleaved giving a single output. Each photo sensor measures twelve micro metres square. The 512 photo sensors are divided into four segments of 128 and are manufactured as follows:

MOS-capacitors with a poly-silicone electrode,

photodiodes with a phosphorus diffusion,

photodiodes with a phosphorus implantation,

photodiodes with a combined implantation: the phosphorus of the channel implant, plus an additional arsenic implantation.

All photodiodes have an additional storage electrode which is between the sensors and the transfer gate. This storage region has its top plate in common with the MOS-capacitor shift registers and acts as a shield.
Two 256 bit CCD shift register are on each side of the sensors, one for the even pixels and the other for the odd pixels. The transfer gate is the link between the sensors and the two shift registers which are controlled by control line "SG". When "SG" is taken to logic "Low", the transfer gate connects the sensors to the shift registers and loads the registers with the gathered charge packets. If this pin is now taken to a logic "High", then the transfer gate will

be open circuit, isolating the two and allowing charge collection on the sensors to re-commence and at the same time, allow the information which has just been placed into the shift registers to be read out. The readout is accomplished by using two, three-phase clocks, one for each CCD shift register, which are 180 degrees out of phase from each other to allowing the output sense diode to alternately receive the charge packets from each shift register as shown in figure 2.2.2. This allows the two outputs to be combined into one.

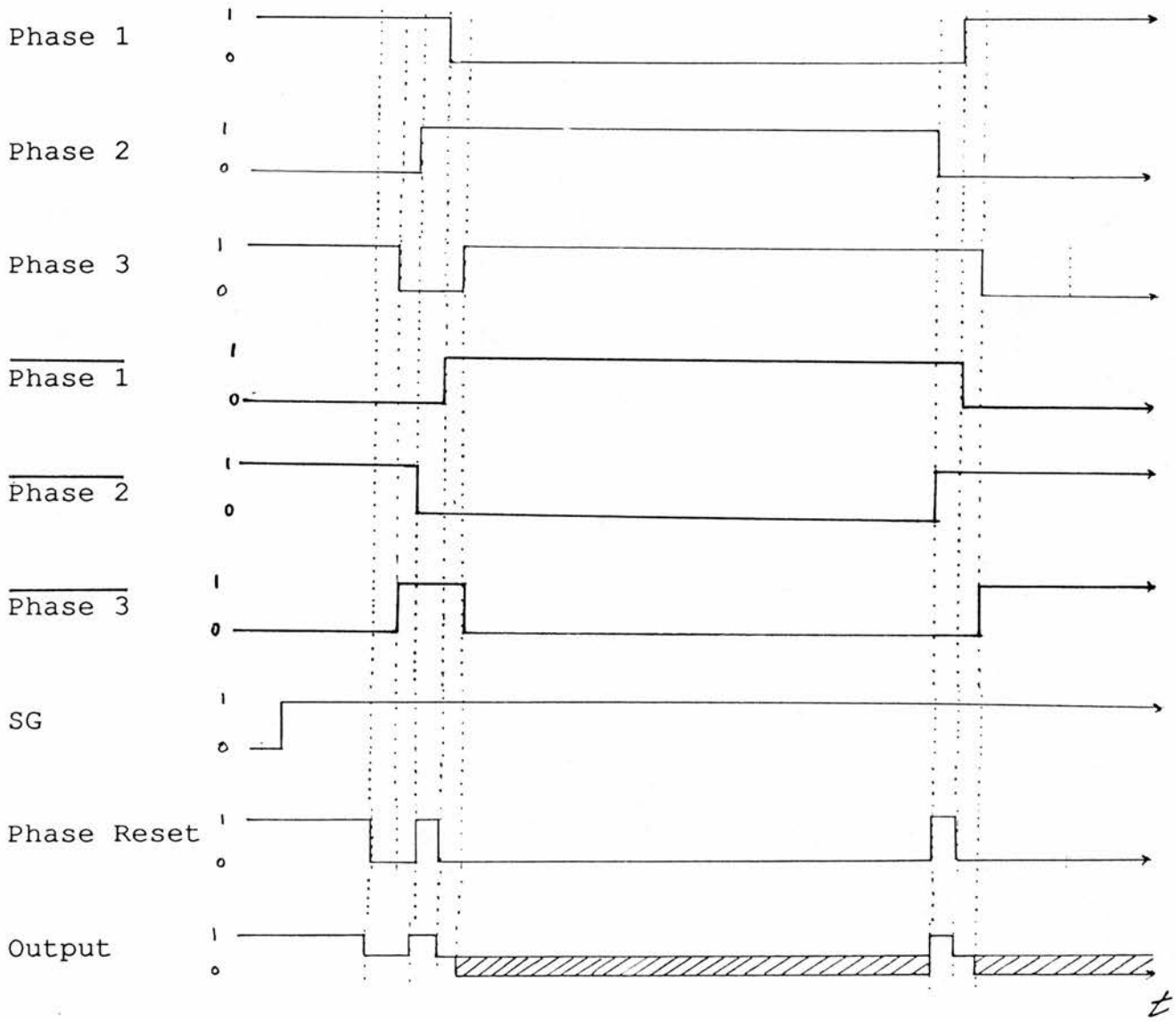


Figure 2.2.2 Three phase timing

The output stage consists of the above mentioned sense diode, a floating gate, a reset transistor and a source follower. The reset transistor discharges the sense diode between charge transfers. The generated potential across this diode is buffered by a source follower and is output on pin "OUT+". Switching noise is picked up in the output stage and is thus present on the output. This noise problem is

overcome with a dummy output stage which only generates switching noise and is output on pin "OUT-". This dummy output stage is constructed from a floating gate, a diode reset transistor and a source follower to be identical to the output stage except that the sense diode is not connected to the shift registers and only picks up noise. When both outputs are used in conjunction with a differential amplifier, the common noise is removed leaving the pure video information.

Figure 2.2.1. are the external connections to the 40 pin ceramic DIL version of the ESA512 CCD IC.

1	Substrate	40	GG Gate gate transistor
2	SF Source field transistor	39	DG Drain gate transistor
3	DF Drain field transistor	38	SG Source gate transistor
4	GF Gate field transistor	37	$\overline{\text{PHASE 1}}$
5	Diode	36	$\overline{\text{PHASE 2}}$
6	$\overline{\text{PHASE 3}}$	35	IN2B
7	DC output plate	34	IN1B
8	OUT+	33	Diode B
9	VDDS for source follower	32	SG Storage gate
10	Drain field transistor.Test	31	
11		30	
12		29	
13		28	
14		27	TG Transfer gate
15	OUT−	26	Diode A
16	Supply for reset transistor	25	IN1A
17	PHASE RESET	24	IN2A
18	PHASE 3	23	PHASE 2
19	POLY capacitor 3	22	PHASE 1
20	POLY capacitor 2	21	POLY capacitor

Figure 2.2.1. ESA 512. Pin identification.

2.3. CIRCUIT BLOCK SCHEMATIC

The circuit has been split into various sections which will now be referred to as blocks. A block diagram of the complete instrument is shown in figure 2.3.1 and only shows the main interconnections between each block and is not meant as a complete interconnection diagram but as a means of understanding the fundamentals of the circuit.

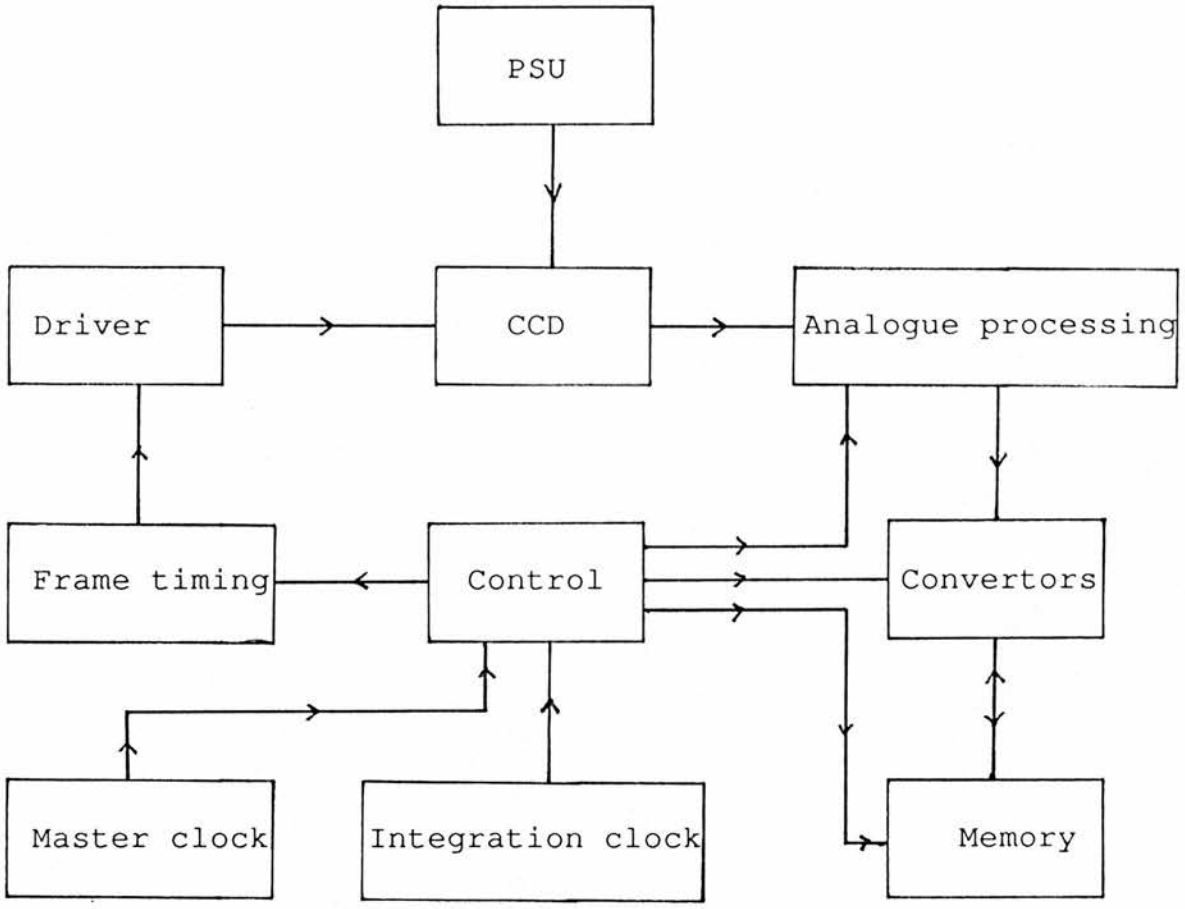


Figure 2.3.1. Driver block schematic

The master clock is the system clock and generates a synchronised 2 MHZ and 1MHZ clock for the sequential logic and convertors.

The integration clock sets the time allowed for the CCD to accumulate a charge on its photo sensors. The repetition rate may be infinitely adjusted on the front panel in the range 2 mS to 50 ms. If desired, an external timing signal may be used instead and would be connected to the external trigger input.

The power supply generates all the required CCD bias voltages and the many other supplies for the analogue and digital circuits with separate signal return paths between them both to keep the logic switching noise away from the delicate analogue signals. This helps to increase the signal to noise ratio of the analogue circuitry.

The control block is responsible for all the back ground timing and synchronising of the whole circuit. These conditions may be altered by the operator by way of front panel switches and external timing signals to suit a particular application.

Frame timing generates the phase timing logic signals to be able to output one complete line of video from the CCD's shift registers and is derived from a look up table ROM which generates all the necessary logic timing waveforms for the CCD and also generates the RAM, A/D convertor, video blanking and end of frame timing signals. A look up table contained in a ROM was chosen for frame timing instead of the usual sequential logic approach since sequential logic circuitry would require a large amount of discreet

logic IC's. For very large quantity production it would be feasible to use a single LSI device but for small quantities the EPROM is the most cost effective and flexible device to implement.

The ROM allows very complex timing sequences to be output with a simple sequential counter rippling through the ROM address range to give eight parallel data output bits. If for any reason the sequencing needs to be modified at a future date, then it is a simple matter to re-programme the ROM with the required bit pattern. Modifying sequential logic would require at least a re-wire or even redesign whereas the EPROM can be erased and reprogrammed with the new bit pattern without any hardware modifications.

The manufacturer's data sheet for the CCD gives a sequential logic circuit suitable to drive the device, however it is unable to ignore the first dummy output from the CCD and misses out the last sensor output. This gave the sequential logic designer a much easier design approach, but with the sacrifice of the first and last charge packet. As phase and memory timing are now held in a look up table, the bit pattern can be incorporated easily into the timing, allowing the first output to be ignored and keeping the remaining sequence in order.

The driver block converts the logic timing waveforms into suitable matched signals that are compatible with the CCD inputs. The CCD head consists of phase timing, pulse shaping and a head amplifier. The components are mounted on a circuit board that are arranged around the CCD, which make up the remote head.

The four types of sensor and the two CCD shift registers all have different sensitivities and offset voltages. The DC offset is most noticeable between the two shift registers and can be of the order of two to three times the size of the output waveform. The gain error can be out as much as 20% between the two CCD shift registers and appears to be a stable characteristic of the devices that were tested. These effects are illustrated in figure 2.3.2. The analogue processing section deals with gain and offset compensation correction to deal with the above mentioned imperfections. The differences between each of the four sensor types is mainly due to the different technologies used in the fabrication and is thus not compensated for.

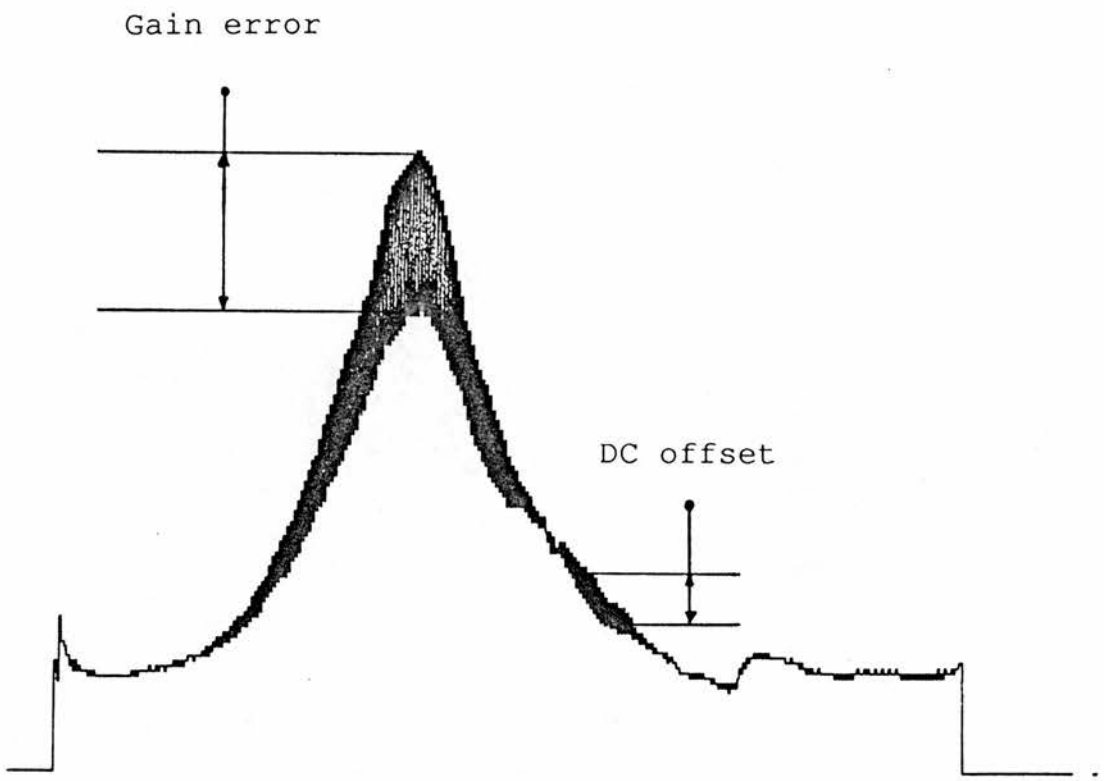


Figure 2.3.2. CCD video output gain and offset errors.

2.4. CIRCUIT DESCRIPTION

2.4.1. Control

The control circuit is shown in figure 2.9.1. Frame timing or "start pulse" is initiated from one of three sources, the internal integration clock, the external input or from a single shot, from the push switch SW2. The latter mode is used to start the sweep for a chart recorder. Switch SW3 selects between the internal or external clock, while SW1a selects the chart recorder mode. Apart for the chart recorder mode, the repetition of the start pulse governs the integration time of the CCD. The integration clock is generated from astable multivibrator circuit of IC106c which is a Schmitt trigger. The output of this clock is buffered by invertor IC106b. The repetition rate of the clock is determined by C100, R100 & P100. The frequency can be controlled by potentiometer P100 from 500Hz to 20 Hz (2mS to 50ms rep rate). The RC network can be calculated from the following equation:-

$$f_I = 2 / R_T * C100 * (1 / \sqrt{2})$$

where R_T is in Ohms, C is in farads and R_T = R100 + P100. Note P100 = 0 for minimum integration time.
The external trigger input is buffered by IC106a and gives high noise immunity with its Schmitt trigger input and is negative edge triggered. R102 prevents latchup when the input is not connected.

The start pulse is connected to the clock input of IC111a, a D-Type latch with the "D" data input tied to logic "High" so that the Q output will be set with a start pulse. The output of the latch is cleared at the end of each frame transfer when frame timing signal "End of frame" goes logic "High" and is connected to the clear input. The "Q" output of this latch is used to reset all counters and is also used as the external oscilloscope trigger which is first buffered by IC106e. The oscilloscope should be set to trigger on the rising edge of this trigger pulse.

The start pulse is also used to clock D-Type latch IC111b to synchronise a "Read" or "Write cycle", to the start of each frame. When changing from a write to a read cycle it is important that the cycle should stop at the end of a frame to prevent partial write cycles. The "D" data input is connected to the "Read/Save" switches SW4 and SW5 and pull-up resistor R103. SW5 is a push switch and SW4 is a toggle switch giving the operator a choice of save mode. Thus, if a write cycle is selected a logic "high" is applied at the "D" input of IC111(b).

D-type latch IC110(a) selects either a fast or a slow counter clock, the latter being used only for slow scan readout of memory for hard copy on a chart recorder. The second pole of SW1(b) in conjunction with pull up resistor R104 sets the logic level on the D input, a logic "High" represents the normal fast clock and a logic "low" selects slow clock, again synchronised with the start pulse on its clock input. The outputs of this latch feed the enables of the master clocks.

The counter clock as described above has an additional slow mode for a chart recorder. This is formed by IC109b, R106 & C101 and its frequency found from the following equation:-

$$f = 1 / R106 * C101 * (1 / \sqrt{2})$$

IC109(b) is a Schmitt input NAND gate with positive feed back on pins 5 and 6 causing oscillation and pin 4 is an enable input. IC109(a) is the fast clock and its frequency set by R107 and C102 with pin 2 as the enable. Hence IC110(a) selects which clock is running at each frame start and gate IC109c presents the clock to JK bistable IC113(a) as a divide by two giving a 50% duty cycle. The clock is then further divided by two by IC113(b) and this forms the analogue to digital convertor clock.

The RAM chip select "CS" input pin 20 is derived from the phase reset signal and only differs in that it is only true for a half clock cycle. D-Type IC110(b) is clocked and is set at a logic "High" by the phase reset signal and reset on the clear input with the counter clock.

2.4.2. FRAME TIMING

The frame timing description is made with reference to figure 2.9.2. Frame address counters IC100 and IC101 are 74HCT4024 7 bit binary ripple counters connected as a 14 bit counter, capable of addressing IC102, a 27C128 EPROM. This EPROM has a capacity of 16K * 8 bits and is pre-programmed with the bit pattern of the frame timing sequence. The

memory is accessed sequentially by incrementing the address counters with the "CK" input and is positive edge active but with reference to "CK" the counters are negative edge triggered. The counters are reset to location zero by the "Frame reset" input going to logic "high".

Due to the address counter outputs being unstable, caused by the ripple through of the internal bistables, this has the effect of producing fast changing address locations which are then output from IC102 data output and are unwanted glitches. IC103 is a 8 bit latch and transfers the input to the output on a positive edge from CK thus latching data when it is stable and then giving a glitch free output as illustrated in figure 2.4.2.

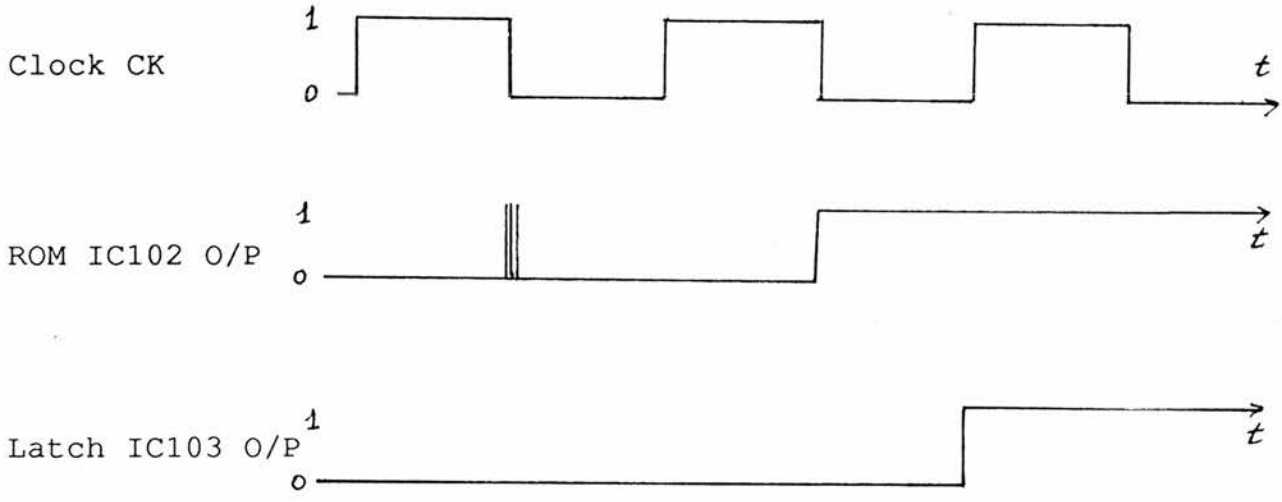


Figure 2.4.2. Frame data timing

2.4.3. MEMORY

The memory circuit description is made with reference to figure 2.9.3. The memory circuit consists of IC108, a 8K * 8 bit RAM IC, IC107 a twelve bit binary ripple counter and a lithium battery for power down memory retention. To prevent memory over-writing when the power supply is switched off, thus corrupting data, the power supply provides a logic signal which goes to a logic "Low" a few milliseconds just before the supply collapses. Also, on power-on, this line will only go to a logic "high" when the supply lines have stabilised. This line is called memory protect and is applied to pin 26 of IC108, the chip enable input "CE".

Address counter IC107 is clocked on the rising edge of "Memory advance" and reset at the end of each frame by IC111(a) pin 6 "Memory address reset" signal. Only the lower 9 bits of the counter are used to select 512 bytes of IC108 RAM. The remaining 4 bits are selected from SW5 thumb wheel switch allowing 1 of the 16 pages to be selected from the front panel at any one time.

Memory protection is achieved with BT1, a 3.6 Volt lithium battery. If a fault occurs and lithium battery BT1 is short circuited, the current will be limited by R110, preventing the battery from discharging its high output currents and causing extreme damage. D102 and D103 are voltage blocking diodes arranged to let BT1 supply only the memory when power is removed and allow the +5 volt line to supply the memory when the instrument is in use. The latter is achieved because the battery is at a lesser potential than the +5 volt supply, thus saving battery drain. The battery has a drain of 2 micro amp from the memory and with its capacity, it will last approximately 5 years (shelf life is ten years).

A write operation is performed when "CE" is logic "High" and both "WR" and "CS" are brought to logic "Low". The data on the data bus is then present on the selected address location of the RAM chip and is latched in when any of the control lines are false but, in this application, the "CS" Chip Select input is used as the control line.

A read cycle is performed when the following conditions are met :-

Write "WR" control line is logic "High".

chip enable "memory protect" input is logic "High".
chip select "CS" is logic "Low".
Data will now be output from the applied address location.
The output will be in a inactive high impedance state when the "CS" input is logic "High" at the end of each frame.

2.4.4. DRIVERS

The driver circuit description is made with reference to figure 2.9.4.

The two three-phase driver inputs to the CCD require a logic "High" of +15 Volts and a logic "Low" of 0V. This is achieved by stepping the logic levels up from TTL levels with a open collector invertor with a pull up resistor to +15 Volts then buffered by IC105(a), (b) and (c) 4049B CMOS buffer invertor to give drive phases 1, 2 & 3 respectively. They are then inverted by the remainder of buffer IC105 to give the three negated phase drive signals.

The CCD reset input is driven from a discrete output circuit. IC104(d) is a open collector invertor with R108 as its pull up resistor. With a logic "Low" input on, IC106d the output transistor of IC104(d) is on, sinking current through forward biased diode D100 with TR100 bottomed. With IC106(d) input at logic "High", IC104(d) output transistor is off and this allows current to flow into TR100 turning it on, sourcing the output to almost fifteen volts. This circuit allows fast switching times. The SG input to the CCD requires a twenty four volt logic "high" level and is driven by a identical circuit as for the reset signal and only

differs by its operating voltage (IC104(e), R109, D101 & TR101).

2.4.5. CCD

The CCD circuit description is made with reference to figure 2.9.5. The CCD and associated components are mounted on a small circuit board as a remote head which is connected to the instrument by way of a ribbon cable and a coax lead, the latter being for the analogue output from the buffer amplifier.

Phase drive signals from the driver are pulse shaped by components C201 through C208 and R204 through R211 and are applied to the phase inputs of the CCD.

Differential amplifier IC205 is configured for unity gain with an input impedance of 7K8 Ohms. The two inputs to the amplifier are fed from the output and the dummy output of the CCD. This removes switching noise and DC bias levels from the CCD. The amplifier has a low output impedance allowing it to directly drive the coax line. The amplifier is de-coupled from the power supply lines by C213 and C214.

CCD IC204 is grounded on pins 1, 25, 24, 34 and 35. +15 volts is applied to the shift register input on pin 33. The supply voltage is fed to IC204 pin 9 and 16. This supply is derived from the +24 volt line via a voltage regulator giving an adjustable voltage over the range +5 to 20 volts by components 78L05, R225, R206, C215, C216. The fixed +5V regulator is able to be varied by lifting the regulators reference pin above ground with reference to its regulated output. Once the output has been set by P206 the output will

remain stable. C215 and C216 prevent the regulator from oscillating.

Pin 27 of IC204 transfer gate requires a preset voltage from 0 to 3V and is derived from a potential divider R213 and P205, fed from the +15 volt line and de-coupled by C211 and C212. The DC output plate pin 7 of IC204 requires a preset voltage in the range 0 to 6V and this is accomplished by potential divider network P204 and R212, fed from the +15 volt supply line and de-coupled by capacitors C209 and C210.

2.4.6. ANALOGUE PROCESSING

The analogue processing circuit description is made with reference to figure 2.9.6. The "Head video" from IC205 is voltage inverted and amplified by a factor of 1.7 by IC206-2 op-amp which is connected as a inverting amplifier. This output is then inverted by IC206-3 with its feedback path directed through IC203, a 74HCT4051 analogue switch connected as a single pole two way change over switch with the centre wiper being "Z" and "Y0" and "Y1" as each pole. The switch "On" resistance is approximately 50 ohms and the applied signal must not exceed + or - 5 Volts. This switch is controlled by a logic input on pin 11 of IC203 with a logic "High" selecting odd pixels and a logic "Low" selecting even pixels. This control signal is generated from the memory address line A0, and thus, on even pixel locations network Z to Y0 is selected and on odd pixel locations, network Z to Y1 is selected. The feedback path for the odd pixel is P202 (Gain), R221, R224 and P201 (DC Bias) this network is connected to the amplifiers output and

has no loading effect on the input when inhibited. The even feedback network is P203 (Gain), R222, R223 and P200 (DC Bias).

The "test head video output" is a buffered version of the "head video" output and is current buffered by follower circuit IC206-4 operational amplifier. This output is uncompensated and is used to monitor the performance of new CCD IC's that are under test.

2.4.7. CONVERTERS

The converter circuit description is made with reference to figure 2.9.7 converter circuit diagram.

The digital to analogue converter IC202 is a Ferranti type ZN428 8 bit digital to analogue converter which takes data from the data bus either from memory or directly from the A/D converter. Data is retained in the converter by means of an 8-bit latch. The latch is transparent when the enable input is logic "Low" and data is held when this input is logic "High".

The converter is a voltage switch type and uses the R-2R ladder network. The output voltage can be calculated from the following formula

Analogue Output = ((n / 256)(V_{RefIn} - V_{os})) + V_{os}

where n is the digital data input.

V_{os} is a small voltage produced by the D/A switch currents flowing through the packaged lead resistance and this is typically 1mV and is small enough to be ignored.

V_{RefIn} is a reference voltage supplied from the A to D converter.

The output is buffered by IC206-1, an operational amplifier connected as a voltage follower with the ADC output feeding the non inverting input via a current limiting resistor R203 which is used for video blanking. The output is then connected to the inverting input and thus the output tracks the non-inverting input. TR1 is used as a switch and is controlled by the video blanking signal to ground the output between frames and gives the operator a visual base for which to reference the DC output level.

IC201 is a analogue to digital convertor type Ferranti ZN439E and uses the successive approximation conversion technique. With chip select at logic "low", conversion is initiated with a falling edge on the "WR" input and conversion is complete within eight to nine ADC clock cycles . The analogue input remains steady over this time from the CCD and a sample and hold circuit is thus not required. Frame timing gives the maximum nine ADC clock cycles required for the conversion to complete before its register is read by RAM and DAC. The data output is double buffered and can be read at any time up to just before the next conversion has been completed. The data output is tristate and is connected straight on to the data bus driving the RAM and DAC when it is selected by "RD" taken low. The analogue input has a range from 0 to V_{ref} (2.5 Volts) and is fed from the analogue processing section.

2.4.8. POWER SUPPLY

The power supply circuit description is made with reference to figure 2.9.8. The power supply is fed from the mains 240V 50HZ supply via a switch and fuse. The primaries of transformer T1, each of 120 Volts, are connected in series and in phase. The mains fuse is a 100mA antisurge type. An anti surge fuse is used due to power up current surges required to charge up the reservoir capacitors as they initially appear as an almost short circuit to the input until they are charged up. This current surge is many times the continuous rating of the transformer and this fuse will allow 20 times its rated current for a few tens of milliseconds before it will blow, allowing the capacitors time to charge.

The power supply generates the following outputs.

+5V at 500mA

+15V at 100mA

+24V at 100mA

-5V at 2mA

-15V at 100mA

Logic level output (Memory protect).

The method used to rectify the secondaries enables the required five output voltages to be generated from a single transformer (T1) with just two secondary windings.

C1, C2 and C3 are reservoir capacitors which are charged via rectifier diodes D1 to D4. Let us consider the charging path for C1 which has the most current drain demand from the circuitry and thus requires fullwave charging. On a positive

half cycle the charging path is through T1d and D1 and on a negative half cycle from T1c and D2 giving the required full wave rectification. C2 is charged on the positive half cycle from T1c and D3. C3 is charged on the negative half cycle from T1d and D4. The secondary voltage waveforms and associated capacitor that is charged is illustrated in figure 2.4.8.

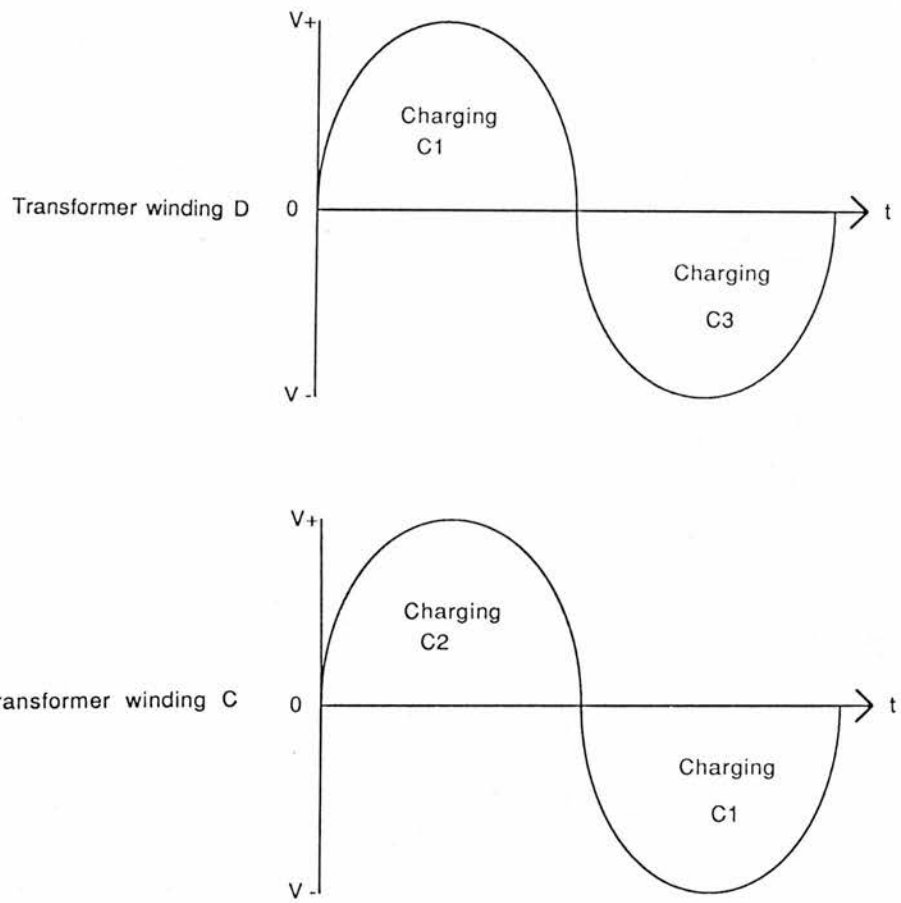


Figure 2.4.8. Reservoir capacitor waveforms

The -5 Volt line is derived from a shunt regulator circuit comprising Zener diode D5 and current limiting resistor R5 and is decoupled by capacitor C13.

The +24, +15, +5 and -15 Volt lines are regulated by series fixed voltage regulator IC's and only require decoupling capacitors on their input and a load resistor and

decoupling capacitor on their output to function. The +5 Volt regulator also incorporates an open collector output that is switched on for a predetermined time after power on and also switches on just before the supply falls. The on time is determined by capacitor C5 and a pull up resistor to the +5 Volt line makes the output TTL compatible. This output is the "MEMORY PROTECT" line.

2.5. SOFTWARE DEVELOPMENT

The frame timing look up table is held on read only memory and its contents were developed on a micro computer system. The ROM used is 16K bytes long and 8 bits wide and is an EPROM type 27C128.

The software to develop the look up table was written in a high level language and the EPROM was programmed with the generated data. The language used was BBC BASIC, run on a "BBC Master 512" in shadow mode allowing all 32K of memory free for BASIC program and 16K of data storage. The generated data was then stored on disc as a continuous data file compatible with the EPROM programmer. The EPROM programmer is a package added to the computer allowing data to be input from disc and programmed onto the EPROM that is plugged into a extension interface card. The programmer incorporates the fast programming algorithm reducing conventional programming times from just under fourteen minutes down to approximately three minutes. Thus ROM's can be developed in a straight forward manner on this very flexible and relatively inexpensive system.

The software to generate the ROM data is listed in figure 2.5.1.

```
0 REM IMEC CCD frame timing ROM data generator. J.M.Wade.
10 MODE 128:REM Shadow memory mode.
20 PROC init:REM Initialise variables.
30 FOR Address% = 0 to 16383:REM 16K address range for data
storage.
40 IF Address% < Start% GOTO 230: REM Oscilloscope delay
50 IF Address% = Start% THEN PReset%=0:REM Clock out first
false pixel.
60 IF Address% = Start%+1 THEN P3%=0    :REM
70 IF Address% = Start%+2 THEN P2%=1:PReset%=1
80 IF Address% = Start%+3 THEN C%=0
90 IF C%=0: P1%=0:PReset%=0
100 IF C%=1: P3%=1:IF LOOP%>1:CounterAdvance%=1
110 IF C%=2: IF LOOP%>1:CounterAdvance%=0
120 IF C%=5: StartConversion%=0
130 IF C%=6:StartConversion%=1
140 IF C%=23: P2%=0:PReset%=1
150
160 IF C%=24: P1%=1:PReset%=0:Videoblancing%=1
170 IF C%=25: P3%=0:CounterAdvance%=1
180 IF C%=26: CounterAdvance%=0
190 IF C%=29: StartConversion%=0
200 IF C%=30: StartConversion%=1
210 IF C%=47: P2%=1:PReset%=1
220 IF C%=47+25: EndOfFrame%=1
230 PROC setbyte:REM Save byte to data address.
240 IFC% >= 0: C%=C%+1: IFC%=48 AND LOOP%<512: C%=0:
LOOP%=LOOP%+2: PRINT LOOP%
250 NEXT Address%
```

```
260 PRINT " '*SAVE "FILENAME" 4000 8000' to save data to
disc."
270 END
280
290DEF PROC init
300 P1%=1:P2%=0:P3%=1:PReset%=1:REM CCD phase drive signals.
310 StartConversion%=1:REM ADC convert command.
320 VideoBlanking%=0:REM Video output enable.
330 CounterAdvance:REM RAM counter advance.
340 EndOfFrame%=1
350 Start%=500:REM Oscilloscope delay before sequence
starts. Even Num.
360 C%=-1:REM Switch off software loop counter.
370 LOOP%=0:REM Switch off software loop counter (-1).
380 ENDPROC
390
400 DEF PROC setbyte
410 REM Set address with all 8 bits with data 2^0 to 2^7
420 Output% = (2^7*P1%) + (2^6*P2%) + (2^5*P1%) +
(2^4*PReset%) + (2^3*StartConversion%) +
(2^2*VideoBlanking%) + (2^1*CounterAdvance%) +
(2^0*EndOfFrame%)
430 Address% ? &4000 = Output%: REM Save data between hex
4000 and hex 7FFF
440 ENDPROC
```

Figure 2.5.1. Frame timing software.

2.6. APPLICATION

As part of the study into diode-pumped solid-state lasers being undertaken within the department, a pulsed-side-pumped laser system has been constructed. This laser uses as its pump source an SDL-922 laser diode array that emits at a wavelength of 810 nm, pulses up to 200 uS long, at between 10 and 100 HZ and up to 25W peak power. The output from the ND:YAG laser when pumped by the diode is typically 0.25 mJ pulses of 150uS duration (1.7W peak power $87KWm^{-2}$ peak intensity).

Of considerable interest in the characterisation of this laser is a measurement of the beam profile. This may be undertaken using a pinhole scan or, much more satisfactorily, using a CCD linear array connected to an oscilloscope. A particular requirement of the drive circuitry for the CCD is that it can be externally triggered by the laser. The beam profile can be noted in figure 2.6.1, the gain drift can be noted as the separation between the scan and increases with intensity.

Difficulties exist in measurement of wavelength for a pulsed laser source. These were calculated in this instance by using a large separation (10mm), plane parallel air spaced etalon with the interference pattern from the diverging laser source and recorded by the CCD. Figure 2.6.1 oscilloscope photograph, shows the laser to be running in 6 modes over an 18GHZ bandwidth.

Fig 2.6.1 Application waveform of beam profile

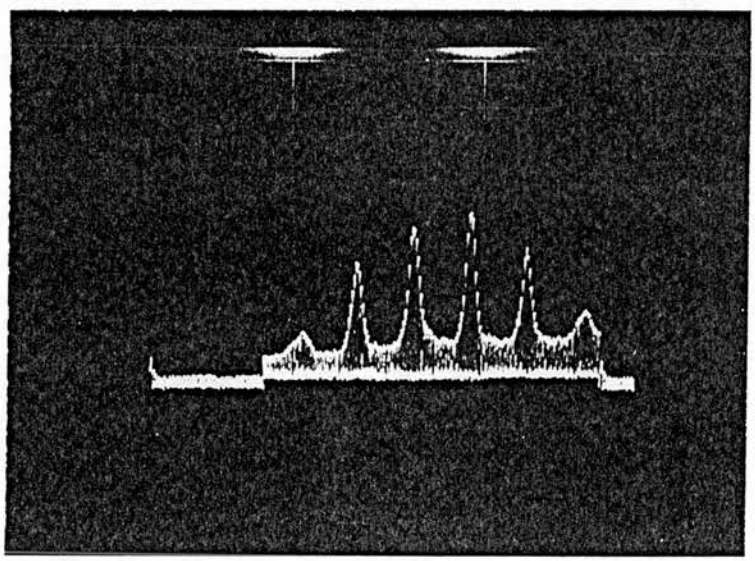


Fig 2.6.2 Application waveform of 6 mode laser source

12.7. CONCLUSION

The frame store has been in use in the laboratory and has proved to perform to the initial design requirements although the grade of CCD has proved to be insufficient for most laboratory work.

Limitations to the instrument lie in the quality of the CCD IC's used. They were only test devices and as such only one in ten possessed the quality for laboratory measurements, but still had the limitation of poor linearity and severe DC drift. The short term drift could be put down to the CCD warming up but the long term drift could not be explained as linearity and DC offset between identical sensor types would alter at different rates, and to a greater extent between sensor types. For future designs higher quality CCD's must be used.

If linearity proves to be a problem, gain and offset values could be held in ROM for each pixel and either corrected for by analogue processing or from a computer. The main problem in the calibration would be generating a uniform light intensity on the CCD with constructive and destructive interference adding to errors. maybe an average level could be read in with the light source being re-aligned for each sample of the average.

2.8. BIBLIOGRAPHY

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Mullard High-speed CMOS logic HC/HCT family. Book 4 1986 ed.

Ferranti ZN439E Data sheet.

Ferranti ZN428E Data sheet.

Signetics L423 Data sheet.

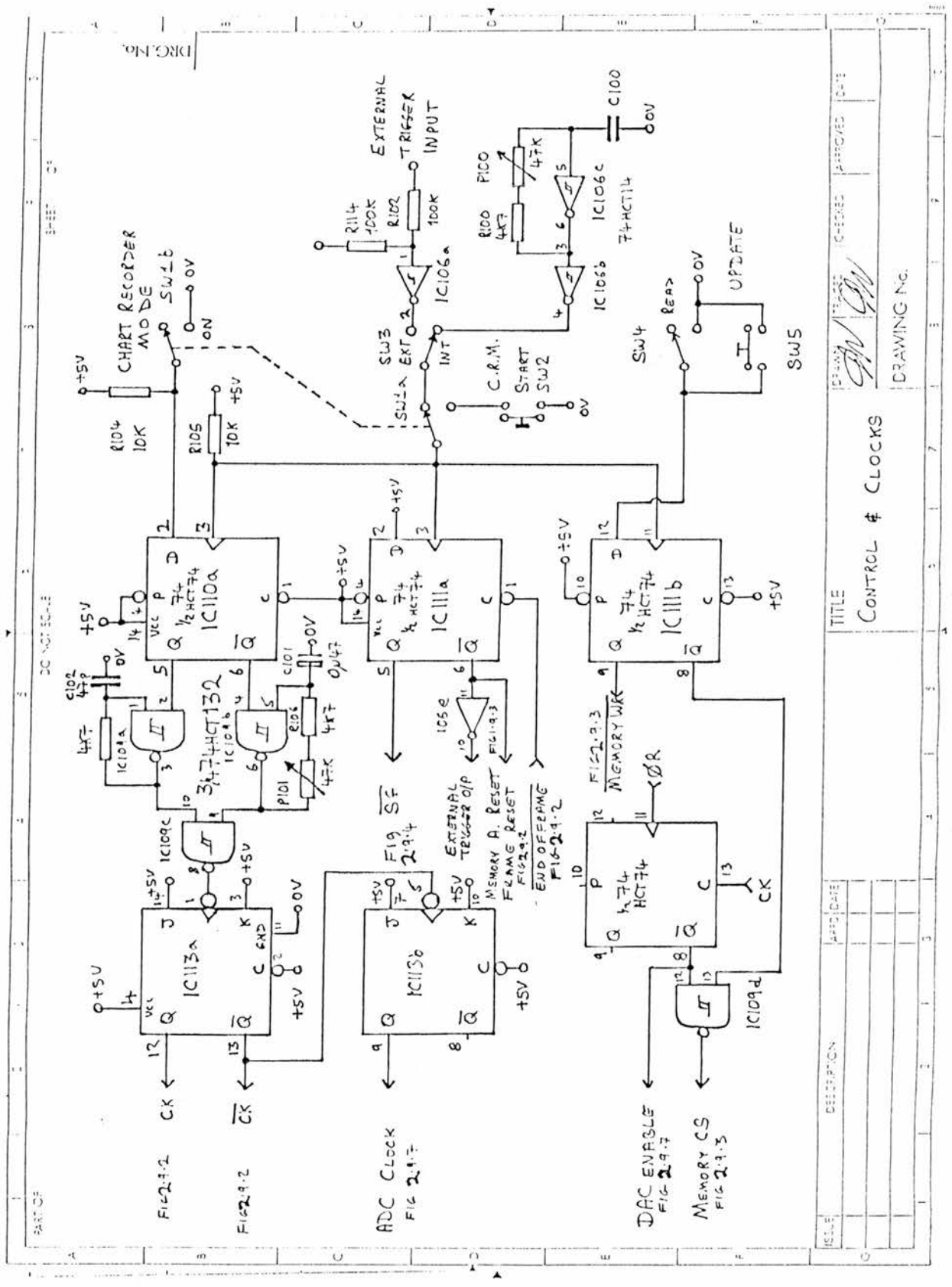

Figure 2.9.1. Control and Clocks circuit diagram.

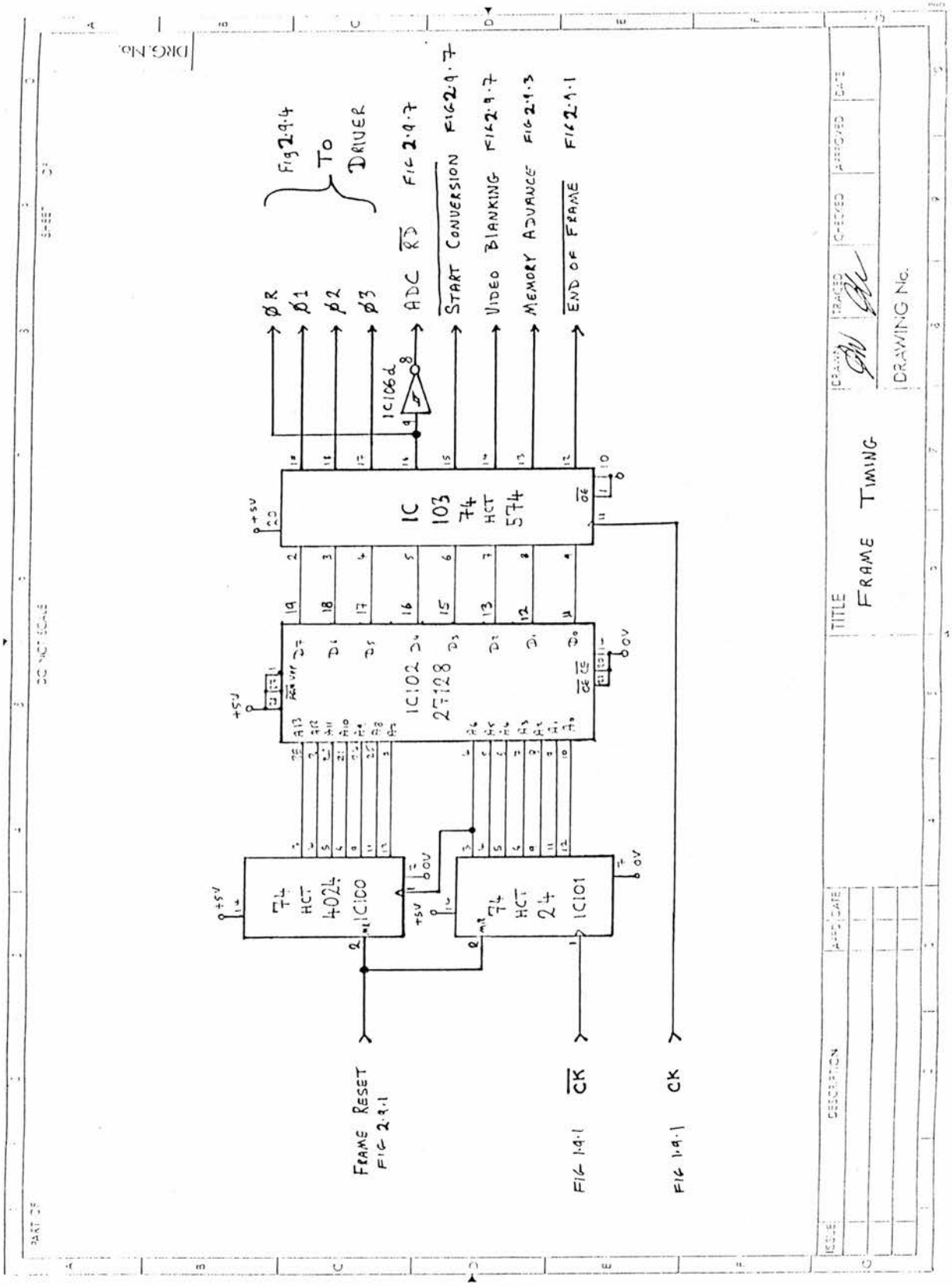

Figure 2.9.2. Frame timing circuit diagram.

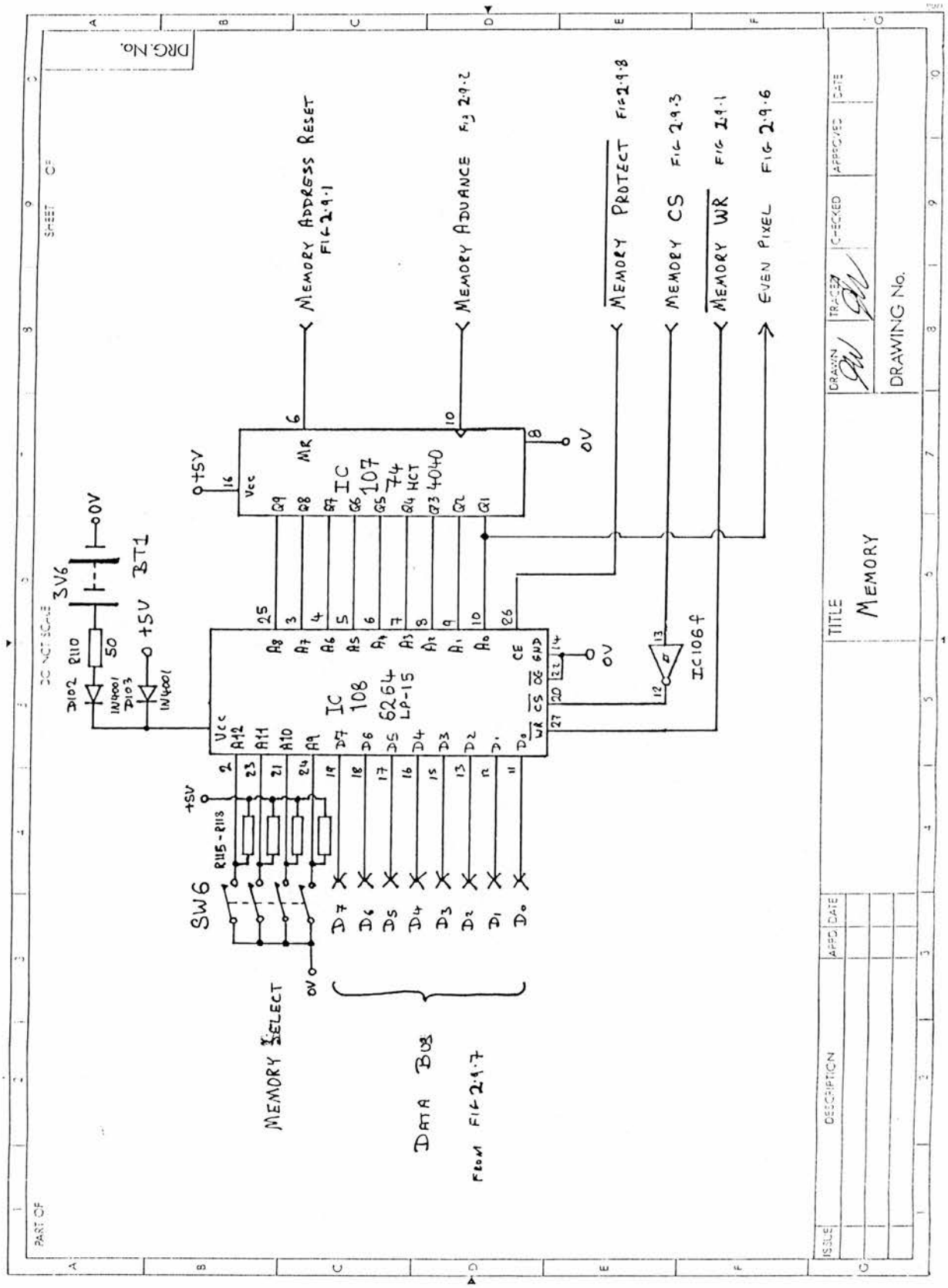

Figure 2.9.3. Memory circuit diagram.

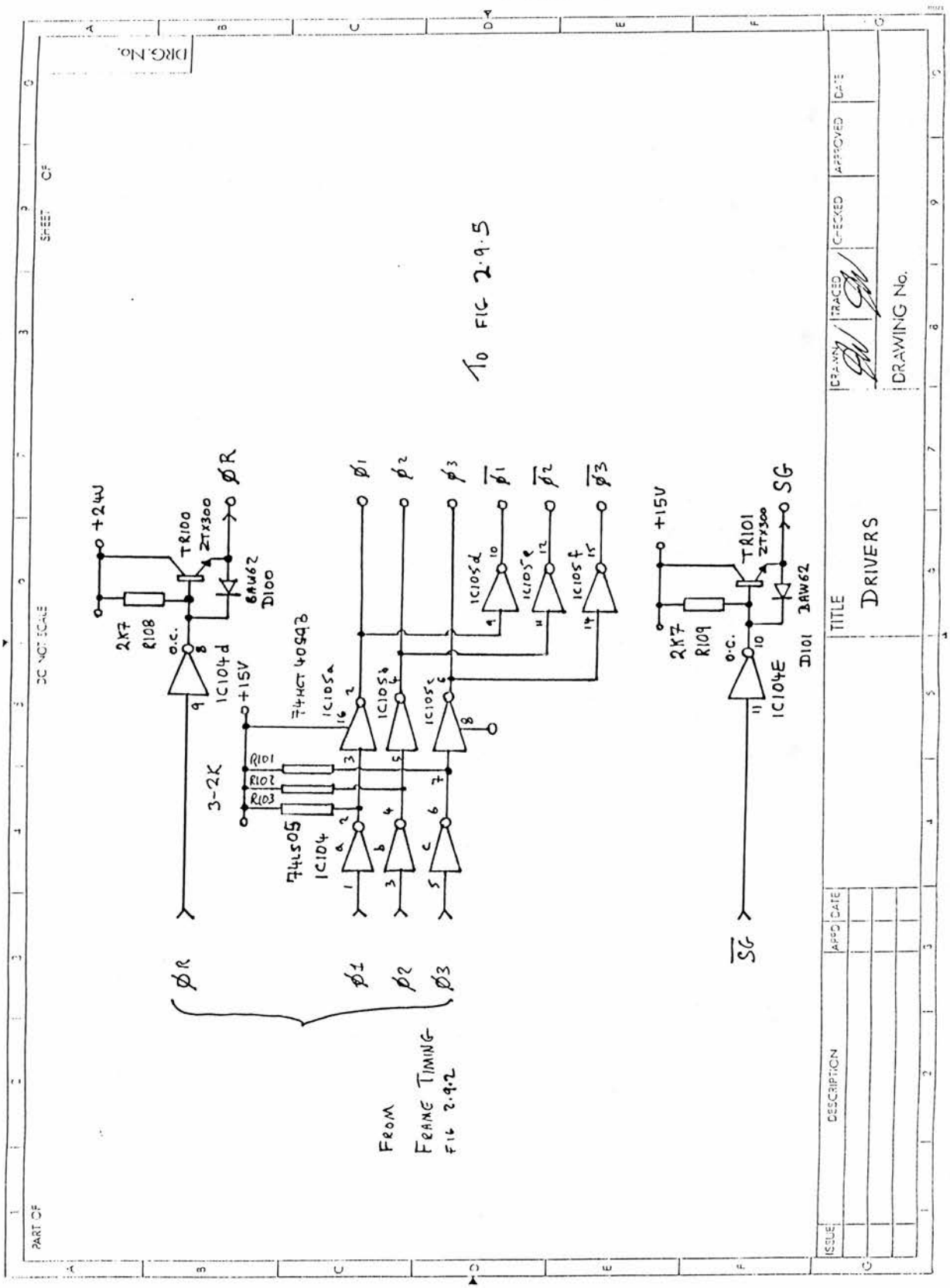

Figure 2.9.4. Drivers circuit diagram.

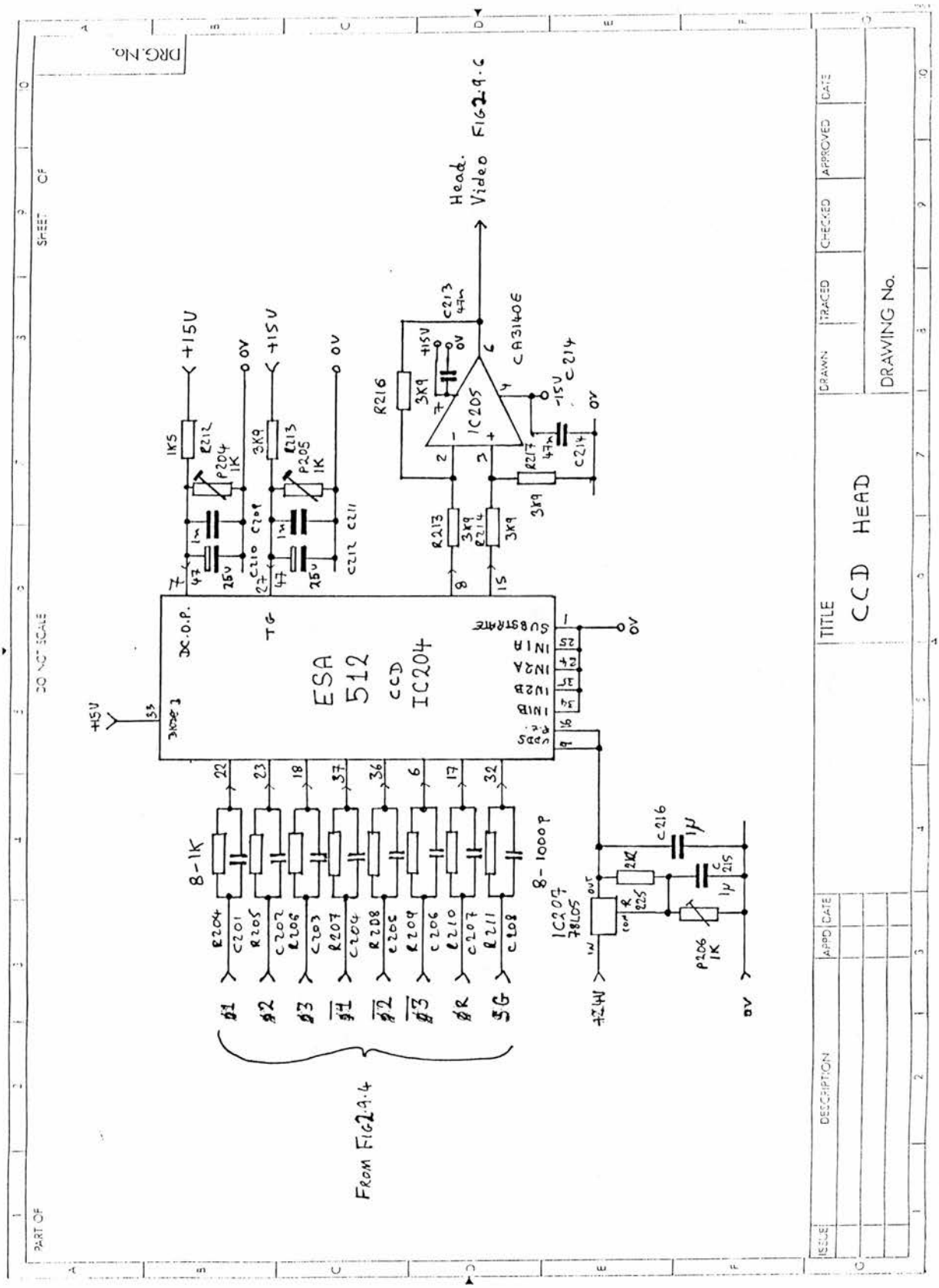

Figure 2.9.5. CCD head circuit diagram.

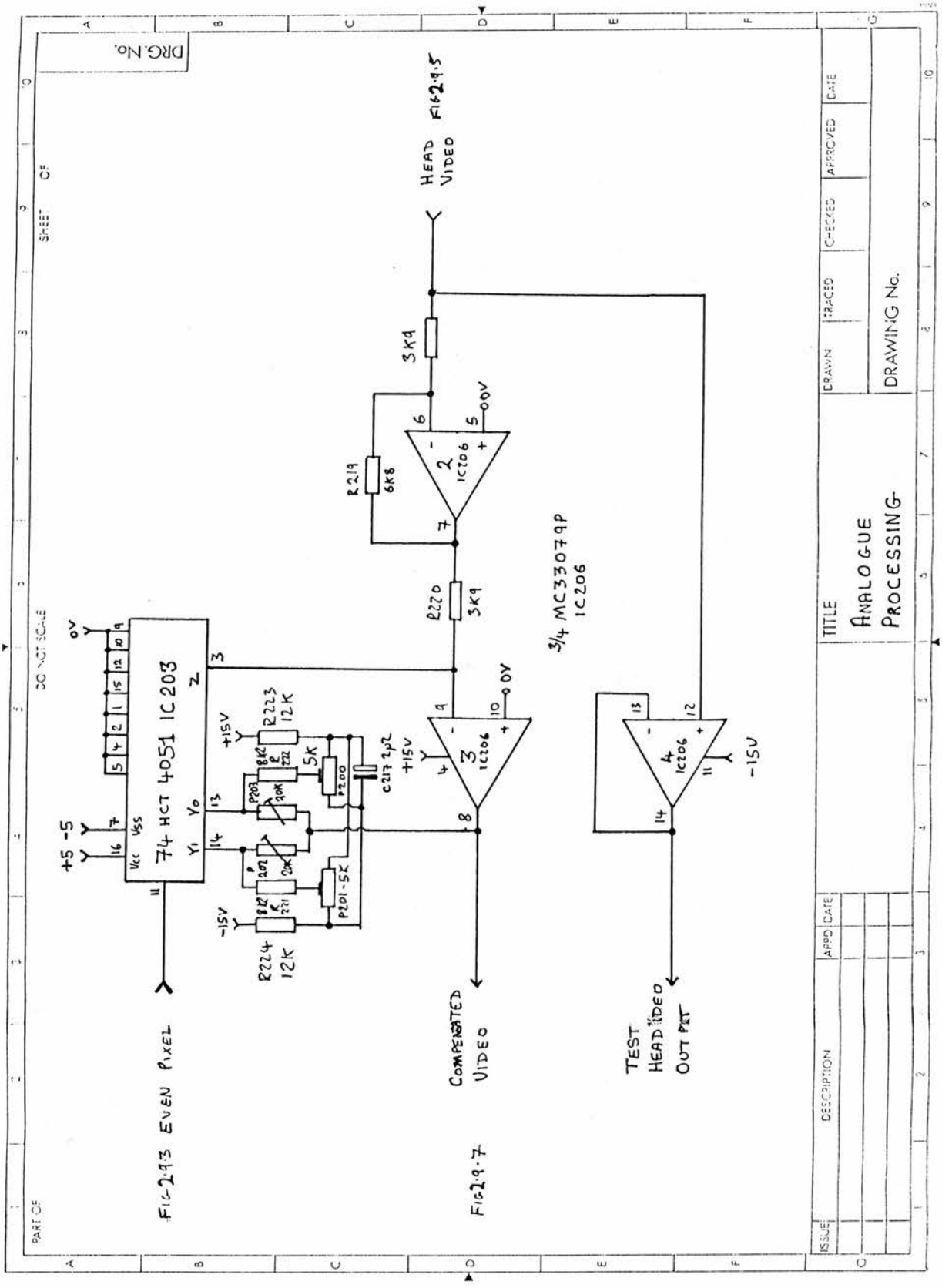

Figure 2.9.6. Analogue processing circuit diagram.

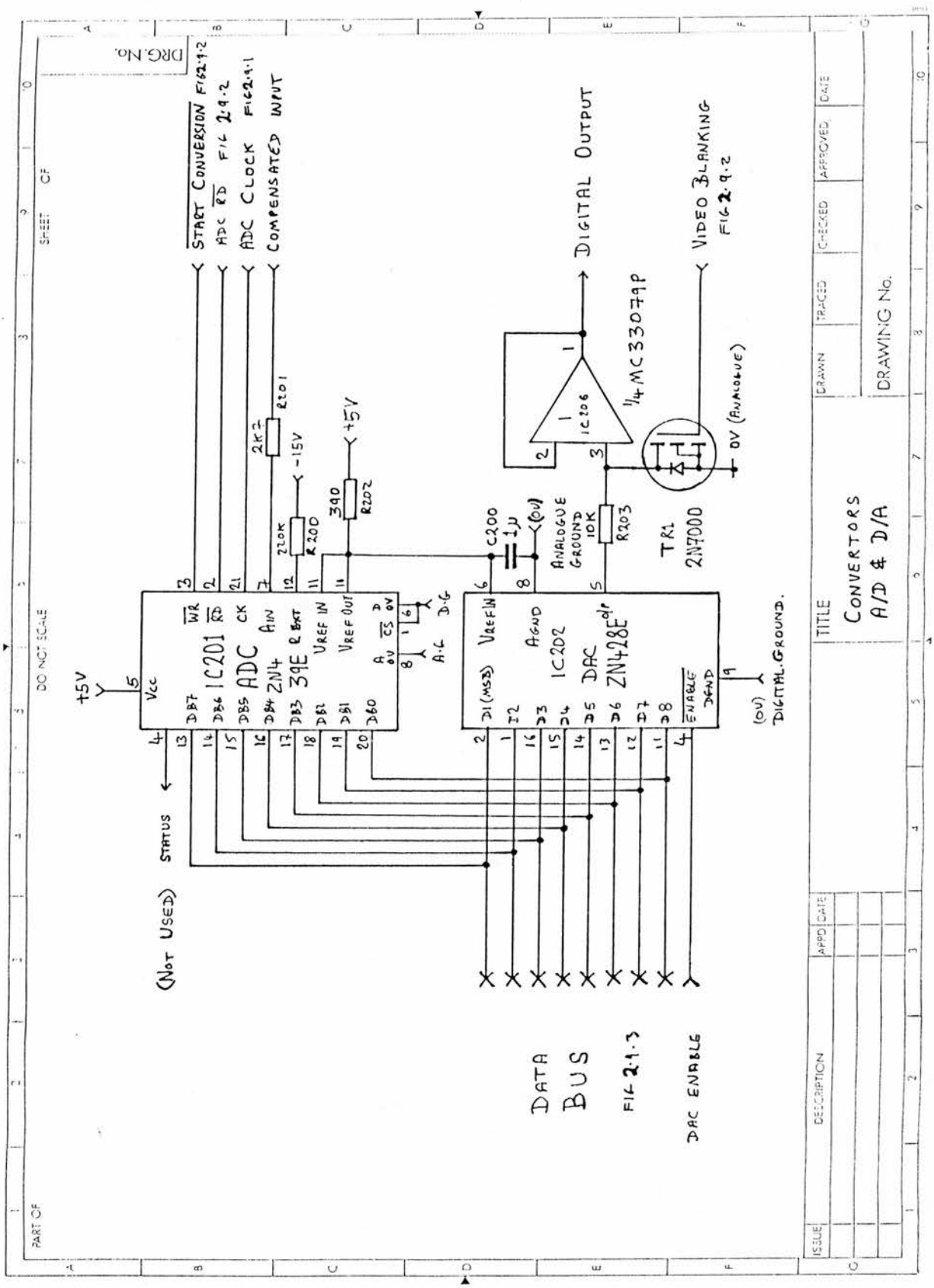

Figure 2.9.7. Convertors (A/D) (D/A) circuit diagram.

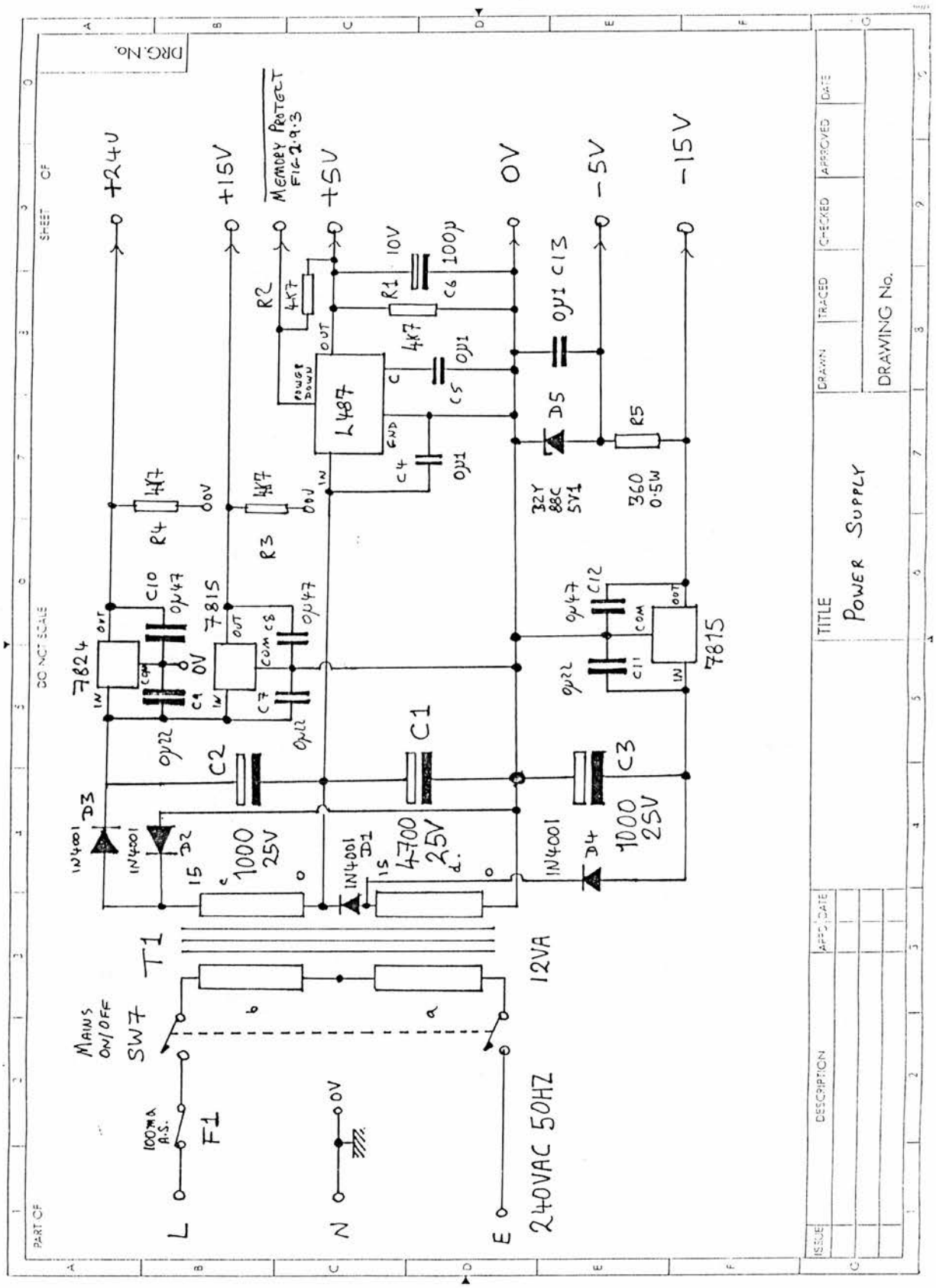

Figure 2.9.8. Power supply circuit diagram.

CHAPTER 3

INTERFEROMETER

CHAPTER 3 INTERFEROMETER

3.1 INTRODUCTION

A high energy nanosecond pulse of light is captured in two dimensions then digitally analysed with this interferometer. The optics for the system were developed by Dr M.Lusty and Dr M.H.Dunn within the Physics and Astronomy department of the University of St.Andrews.

The light source to be analysed originates from a Quantel ND:YAG pulse laser. This beam is passed through the specially developed optics to produce a interference pattern, this two dimension single and short duration image is the input to this system. This chapter deals with the development of this hardware.

An image of short duration is captured on a 2-dimension CCD within a single video frame. The frame is then digitized and stored indirectly to the memory map of a micro-computer allowing complex data analysis to be carried out at leisure.

The video frame is digitized on a video frame grabber and was built from a 'Electronics and Wireless World' design which was adapted and modified to interface on to the Acorn Computers 1MHZ Bus of the Archamedes microcomputer.

The laser, CCD video camera and microcomputer are driven from separate clock's and circuitry was developed to monitor all three and generate a control signal when there was a coincidence. The computer can then generate a start pulse at leisure thus giving it master control to request the start of a frame grab. When this request is given the interfacing circuitry waits for a trigger from the laser and the camera is integrating an image, before the frame store is requested to grab. This prevents an image being captured

during the cameras frame transfer period and if captured would produce false data, if this has happened then the process is repeated until the timing occurs at the required interval.

3.2 CIRCUIT BLOCK SCHEMATIC

The block schematic for the complete system is illustrated in fig 3.2.1. The heart of the system is timing control. When on request from the microcomputer for a new sample, the timing control is armed and then on a laser trigger pulse coinciding with the CCD camera integrating, the control unit then forces the frame store to grab the next video frame output from the camera.

The frame grabber as its name suggests captures a complete frame in a single action. With a definition of 512*512 pixels and resolution to 7 bits. It has three modes of update (a) the video RAM is continuously updated, (b) a freeze mode and (c) where the microcomputer feeds the video RAM with an image. A real-time digitized output is available to allow the monitoring of the video RAM in high resolution.

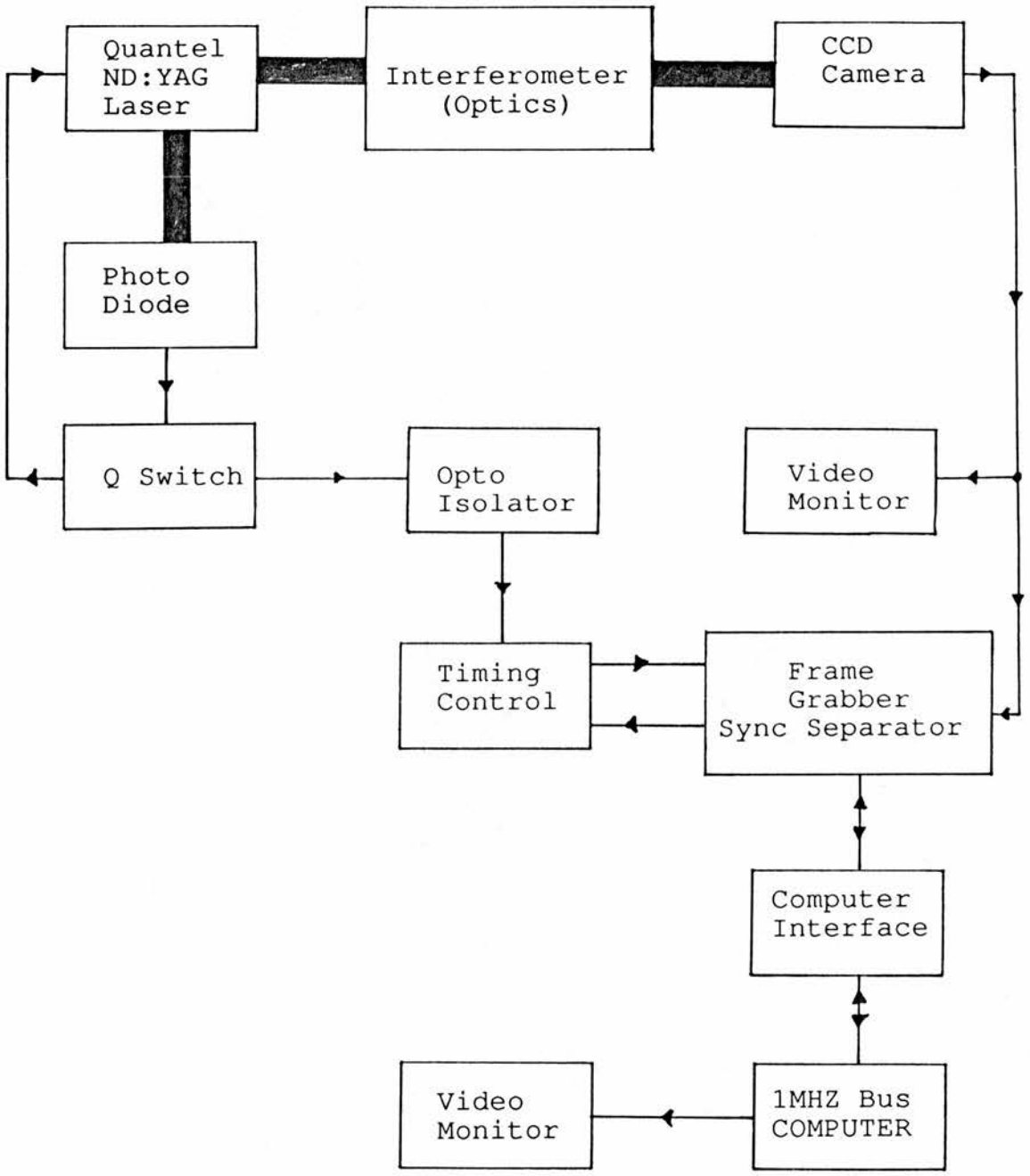

Figure 3.2.1 BLOCK SCHEMATIC

3.3 CCD CAMERA OPERATION

The CCD video camera is a Philips 56470 utilising a frame transfer CCD, type NXA1011.

The CCD works on the frame transfer principle, according to which each field of the complete picture frame is separately integrated within a photosensitive imaging region, transferred by CCD shift registers into a storage region during vertical blanking, and then clocked out serially to form the video signal during the subsequent field integration period.

The CCD uses recent MOS techniques to produce the VLSI necessary to produce a large chip with a imaging region with a 7.5mm diagonal and comprises of 294 lines, each containing 604 pixels, with a pixel size of 10um x 15.6um

Figure 3.3.1 illustrates the FT (Frame Transfer) structure. It is made up of a photosensitive imaging region next to a storage region and connected to it by 604 parallel CCD shift registers. These registers are separated by stop diffusions and their width defines the pixel width.

A two dimensional charge pattern representation of the image to be televised is integrated in the imaging region over the duration of a field (20ms) and transferred to the storage region during the vertical blanking period.

Figure 3.3.2 shows the FT structure in more detail. The CCD is made up of pixels with 4 electrodes enabling a balanced interlaced television compatible output. Other 3 electrode television CCD's use two electrodes to store the charge on each field which gives an imbalanced interlaced video output. This CCD uses three electrodes to store the

charge on each field, thus giving a balanced charge collection between interlaced fields. The imaging and storage regions are practically identical, both being based on four-phase CCD shift registers (phases I1 to I4 as the integration region and S1 to S4 as the storage region).

Charges generated by incident light in the imaging region are collect beneath the gate electrodes with the application of a high potential. A low-potential electrode repels them, thus forming a boundary between charge packets to produce the individual pixels (charge collection cells).

Fig 3.3.2 also shows the horizontal read-out structure. This comprises of three three-phase horizontal CCD shift registers controlled by gate electrodes 1G, 2G and 3G. The pixels in each line are thus read out in groups of three as indicated in figure 3.3.2, selection being controlled by three transfer gates TG1, TG2 and TG3.

This provides two advantages. First, it allows a much higher horizontal pixel density than would a single read-out register, in which the finite width of the gate electrodes limits the minimum horizontal spacing between charge packets. With three shift registers, this spacing is effectively reduced threefold.

The first field is generated when the phases 4, 1 and 2 are HIGH (positive voltage) and 3 is LOW (approximately 0 volts), Figure 3.3.3(a). Phase 3 effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath 4 to 2, centred on 1.

So each pixel extends vertically over roughly three gate electrodes.

The potential distribution of the second field and hence its position relative to the first field is shown in figure 3.3.3(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on 3 and with 1 forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

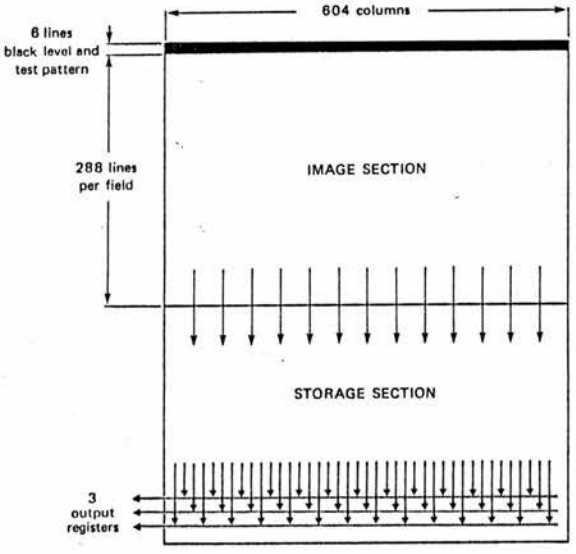

Fig 3.3.1

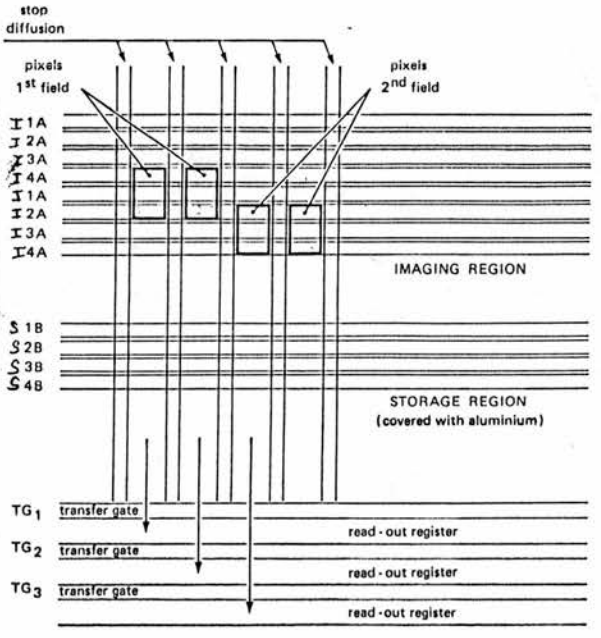

Fig 3.3.2

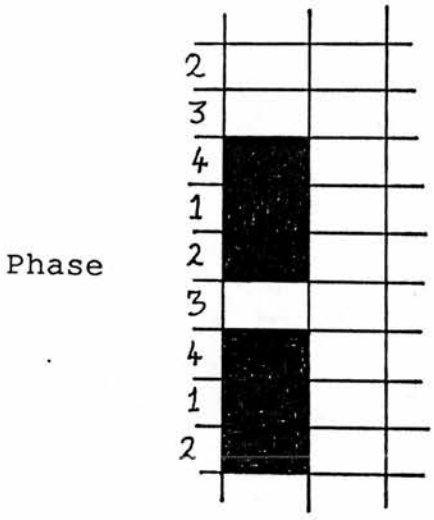

Fig 3.3(a)

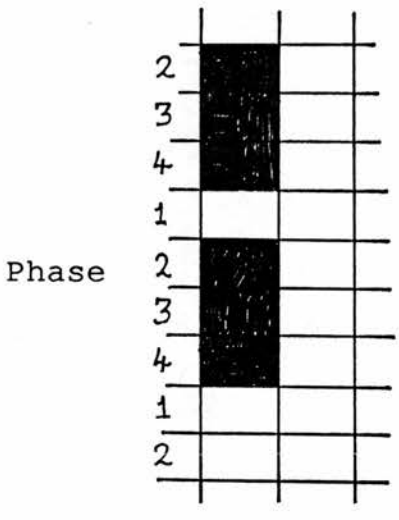

Fig 3.3(b)

3.4. CIRCUIT DESCRIPTION

3.4.1 1MHZ BUS INTERFACE

The 1MHZ Bus Interface of a BBC microcomputer comprises of a buffered databus and the lower 8 bits of the microcomputers 16 bit address bus together with control signals. The bus is illustrated in figure 3.4.1.1 with a description of each pin to follow :-

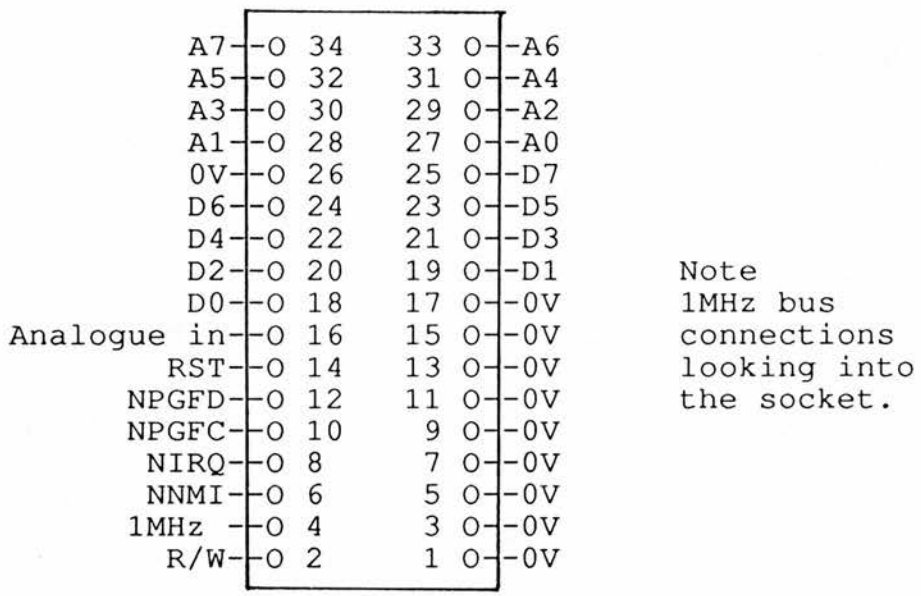

Figure 3.4.1.1. The 1MHz Bus Connector.

0 Volts. This is connected to the main system 0 volts line.

R/W. This is the read-not-write signal from the 6502 CPU, buffered by two 74LS04 inverters.

1MHz. This is the 1MHz system timing clock. It is a 50% duty cycle square wave. The 6502 CPU is operating at 2MHz, so the main processor clock is stretched whenever 1MHz bus peripherals are being accessed.

NNMI. Not Non-Maskable Interrupt. This is connected directly to the 6502 NMI input. It is pulled up to +5 volts with a 3K3 resistor.

NIRQ. Not Interrupt Request. This is connected directly to the 6502 IRQ input. Any devices connected to this input should have 'open collector outputs'. The line is pulled up to +5 volts with a 3K3 resistor.

NPGFC. Not Page FC(hex). This signal is derived from the 6502 address bus. It goes low whenever page FC(hex) is written to or read from. FRED is the name given to this page in memory when referred to in the computer reference manuals.

NPGFD. Not Page FD(hex). This signal is derived from the 6502 address bus. It goes low whenever page FD(hex) is accessed. Jim is the name given to this page in memory.

NRST. Not Reset. This is an active low output from the system reset line. It may be used to initialise peripherals whenever a power up or a BREAK causes a reset.

Analogue input. This is an input to the audio amplifier on the main computer which drives the internal loudspeaker.

D0 - D7. This is a bidirectional 8 bit data bus which is connected via a 74LS245 buffer to the CPU. The direction of data transfer is determined by the R/W line signal. The buffer is enabled whenever FRED or JIM are accessed.

A0 - A7. These are connected directly to the lower 8 CPU address lines via a 74LS244 buffer which is always enabled.

The standard uses of this versatile bus allow up to 64 K Bytes of paged memory as well as 255 memory mapped input-output address locations (plus the paging register). Page FC (Hex) is assigned as the memory mapped I/O page, page FD (Hex) is assigned as the 64K memory expansion paging register. The hardware is thus mapped onto the I/O page and this page has been allocated to various peripheral devices by Acorn Computers and the most suited address space for this application is F0 and F1 (Hex).

On the control bus there is a decoded output for Page FC (Hex) called NPGFC. This control line is active logic "low" but also pulses (glitches) appear when the processor address bus changes between machine cycles and these glitches must first be removed with a latch circuit. The bus waveforms and deglitched page select waveform are shown in figure 3.4.1.2. The clean-up latch circuit comprises of IC4B, IC5A and IC2F from figure 3.4.1.3. When page address FC(hex) is selected from software, its decoded control line

(NPGFC) goes active logic "low" just after the Clock (1MHZ) goes to logic "high" and remains logic "low" through the next clock rising edge, D-type register IC4B then latches the logic "low" signal from NPGFC. The output is cleared when the clock returns to logic "high" which is also fed to the latches preset input. Feedback from the Q output to the preset input is used for power on resetting of the latch via NOR gate IC2F.

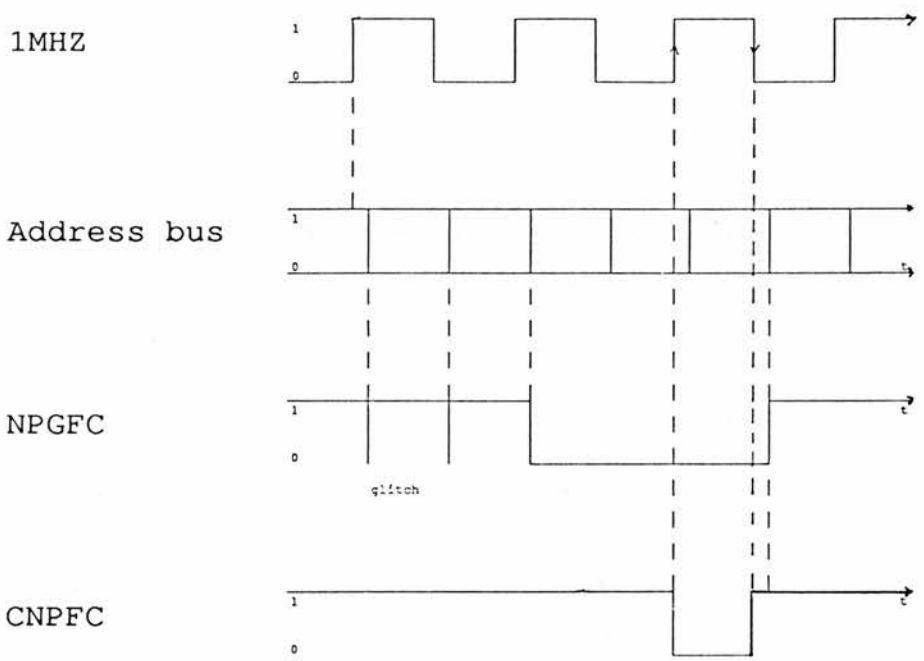

Fig 3.4.1.2. 1MHZ Bus clean-up circuit timing diagram.

IC1 decodes the lower 8 bits of the address bus and is a 8 input NAND gate. Bits A1 to A3 are negated, and A4 to A7 connected directly, thus decoding addresses F0 and F1 (Hex). The deglitched page select is used to enable IC1 to give the overall decoded address locations for FCF0(Hex) and FCF1(Hex).

IC3 is a 2 to 4 line decoder with the output of IC1 as its enable. The other inputs to IC3 are address A0 and the Read/Write control line, generating two read register selects and two write register selects. These 4 outputs are the chip select lines and are active logic "low".

The frame store requires a bidirectional data bus, seven output control bits and a single input bit while timing control requires one input and one output line. Thus one input and one output port is required, along with a bi-directional data bus.

The write cycle timing to transfer data from the computer to the output port latch is shown in figure 3.4.1.6. The active timing point for the data to be written is on the leading edge of the "chip select" line.

The read cycle timing to transfer data from the input port into the computer is shown in figure 3.4.1.5. The active timing point being the trailing edge of the chip select line.

Input and output buffers are shown in figure 3.4.1.4. The output port is implemented with a 74HCT374, an 8 bit latch. Data is latched from the computer with a rising edge on its clock input (pin 11). The chip select line from IC3 pin 15 falls at the required time but, being the wrong edge, inverter IC2D is used to negate this line.

The input port uses a 8 bit tri-state buffer. The outputs to the 1MHZ data bus are active when 'OE' pin's 1 and 19 of IC7 are taken logic "low". The chip select is derived directly from the address decoder (IC3 pin 14). Thus

when this address location is read from the computer the current frame store data bus is read.

The bi-directional data bus is implemented using the same devices as the input port and output port except that the frame store side is wired together. Contention of these logic lines is prevented by the software driven control line (write enable control line) on IC9 pin 2, which drives the output enable of IC8, preventing bus contention.

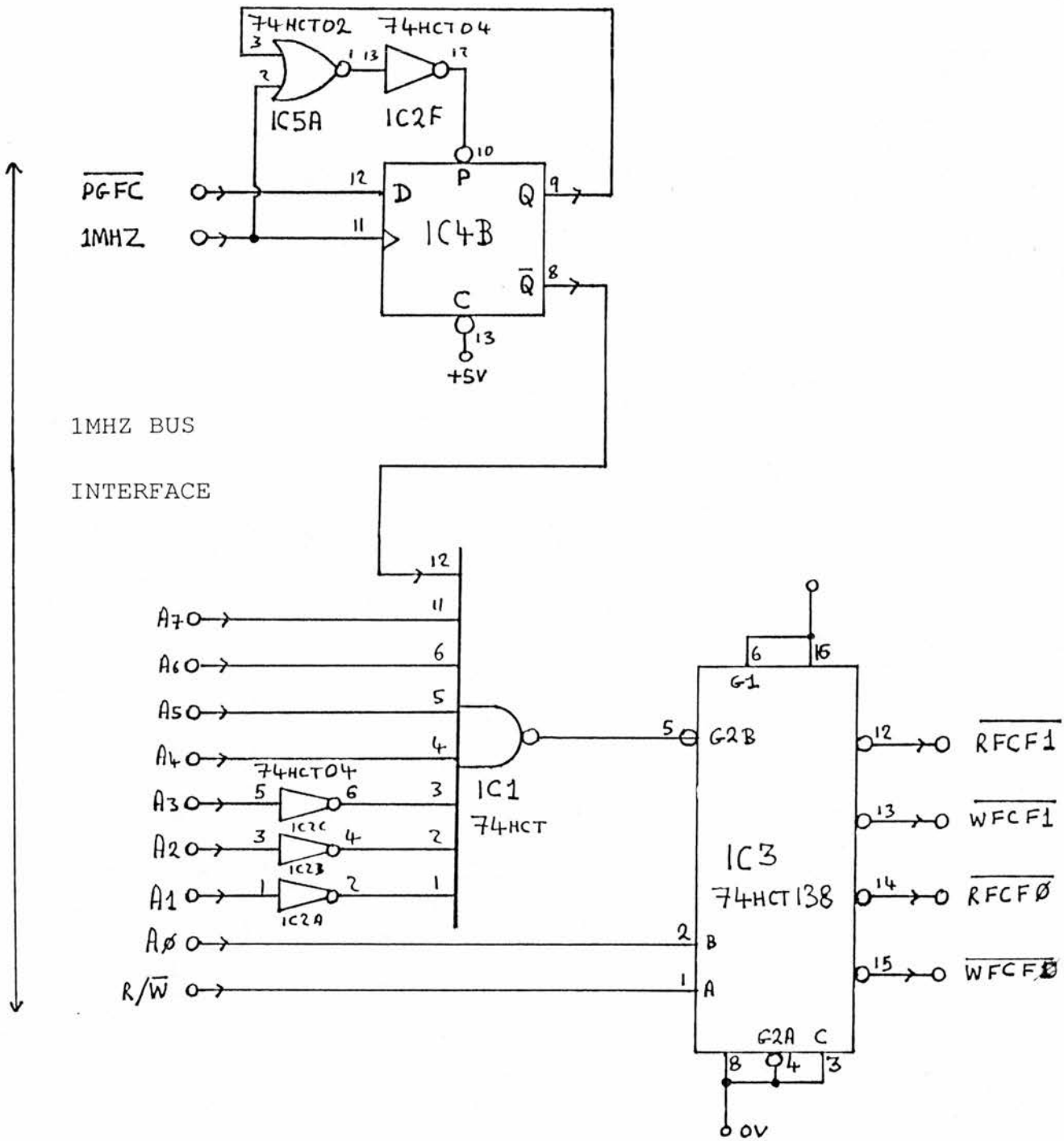

Figure 3.4.1.3 1MHZ Bus decoder

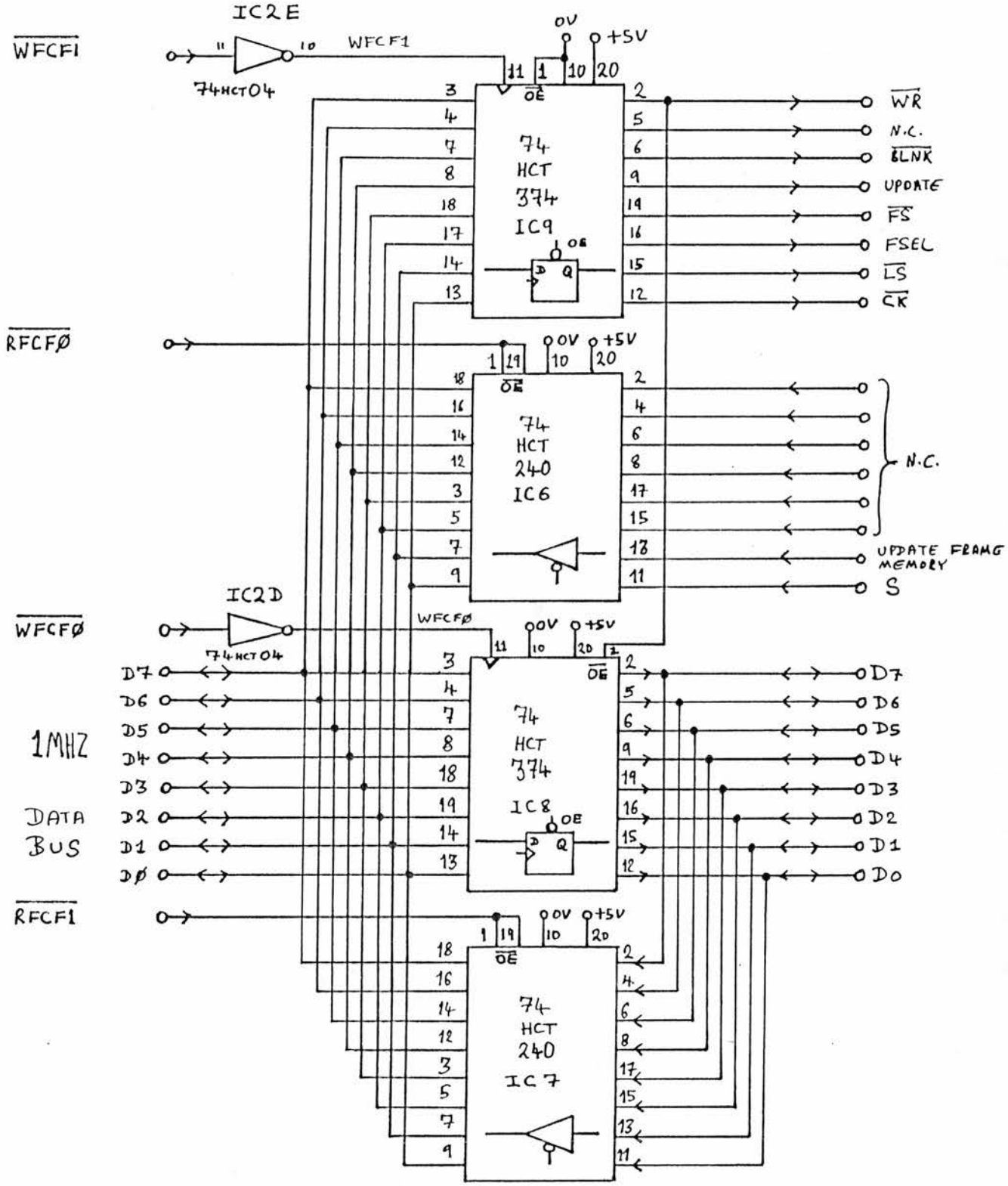

Figure 3.4.1.4. 1MHZ Bus data buffer

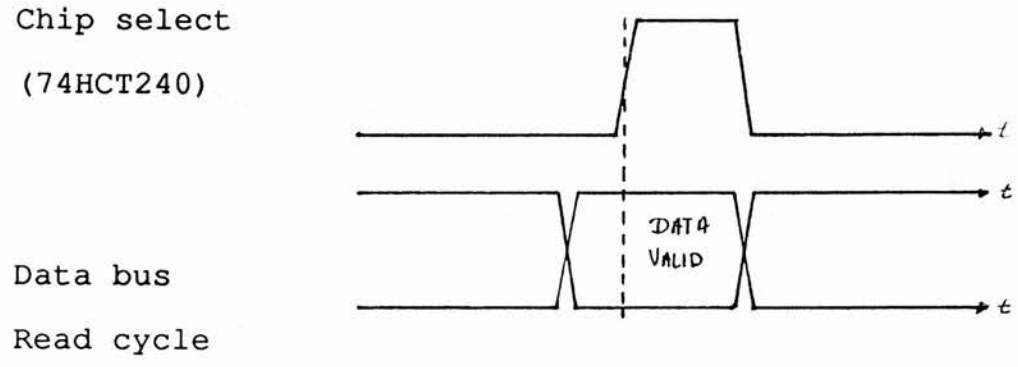

FIGURE 3.4.1.5. Read Timing Cycle

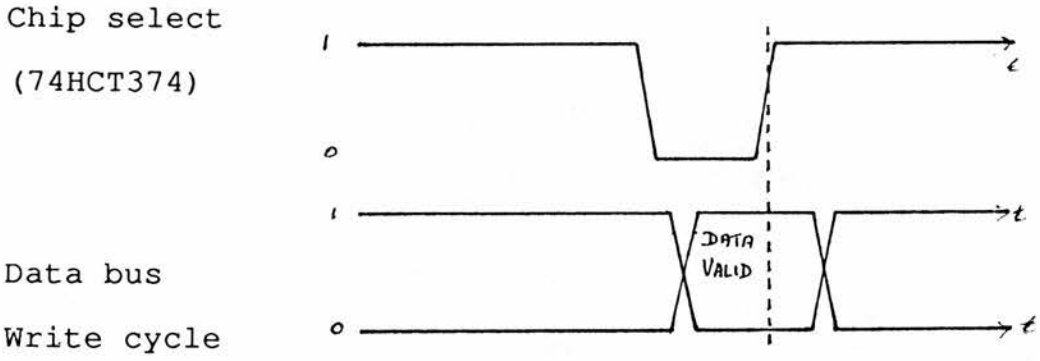

FIGURE 3.4.1.6. Write Timing Cycle

3.4.2. TIMING CONTROL DESCRIPTION

When requested from the CPU to digitize a video frame with the "update signal", the timing control is responsible for applying the correct waveforms to the frame store to digitize the next video frame out of the CCD camera after a valid laser pulse has occurred. Timing control must then wait a frame before digitizing commences to synchronise to the correct video frame.

An opto-isolated TTL logic signal from the laser Q-switch indicates that the laser has fired with a short logic level pulse. This signal is used to clock a D-type register IC4A (figure 3.4.2.1). The data input of this register is fed from the field sync generator of the frame store. If the video sync is valid when a pulse is received from the Q-switch then the D-type registers Q output will be set to logic "high" and indicates a freeze frame. Since the frame to digitize is still held within the CCD itself then the present frame must be output first. This is accomplished conveniently since the frame store will only digitize the next complete video frame, and thus the required CCD image will be digitized. Feedback is used on the D-type register by way of NOR gate IC5C to prevent multiple updating. This whole process can be repeated by toggling the "update" line from the computer which enables the D-type register on its clear input, initiating a new frame transfer.

from the computer which enables the D-type register on its clear input, initiating a new frame transfer.

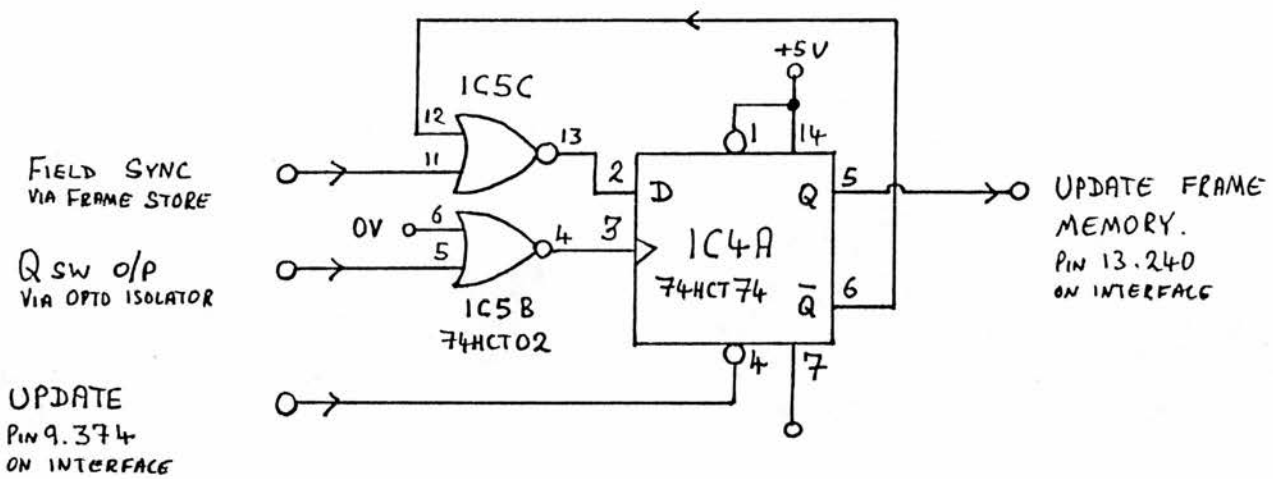

Figure 3.4.2.1 Timing control

3.5 HARDWARE

The 1MHZ bus interface, timing control and frame store are all contained within a single instrument case which adds to the stability of the system. The system is running in a hostile environment in that the laser runs from a three phase supply and the laser is a pulsed type, emitting high EMR. The use of the opto-isolator between the laser system and the computer, prevents earth loops which in the prototype system was able to cause false data and to even crash the computer in some instances.

3.6 SOFTWARE

This is the program used for the frame store control and data processing necessary for beam profile analysis.

The frame store is driven from BBC BASIC with RISC (Reduced Instruction Set Computer) 32 bit machine code subroutines that are used for fast data access and the BBC Basic for complex data analysis.

The microcomputer was chosen due to its high processing speed with its 32 bit processor and 1 Mega-byte of RAM of which a video frame requires 128K bytes of storage area.

Line number's 110 to 260 contain the main program loop which scans the keyboard function keys for a subroutine request and then initiates the relevant subroutine. When the requested subroutine is finished, control is then given back to the main program loop again.

Line numbers 280 to 660 are the hand-shaking and general frame store house-keeping routines.

Line's 650 to 950 are the RISC machine code routines used to input data from the frame store and "pseudo-colour to grey scale conversion" for the graphics display.

From line 970 onwards are Dr M.Lusty's data processing routines.

The program is listed in figure 3.6.1(a) through (d)

An understanding into the programs user-interaction is probably best described by considering two examples. In the first a single frame of video is captured, read into the computer, and a simple scan of intensity verses position of a segment of the picture is displayed (Figure 3.7.1) and then printed out on a dot-matrix printer. In the second

example the procedure for obtaining an elliptical scan is described.

Figure 3.6.2 describes briefly the function keys operation.

Example 1. Steps to obtain a 5 line average

i) Reset framestore (F1)

ii) Sample picture (F2)

iii) Perform linescan (F7)

iv) Display linescan result (F3)

v) Screen dump of result

vi) Reset framestore (F1)

Example 2. Steps to obtain an elliptical average of intensity / position

i) Reset framestore (F1)

ii) Sample picture (F2)

iii) Convert to black and white picture (F8)

iv) Position ellipse to obtain ellipse equation (F9)

v) Resample picture (F2)

vi) Execute elliptical averaging

vii) Display elliptical scan results (F3 of F10)

iix) Screen dump of result (F12)

ix) resample picture (F2)

x) Save picture to disk (F5)

xi) Reset framestore

```
    2 REM Computer Aided Interferometer Algorithm
    4 REM
    6 REM                          MICHAEL LUSTY + JAMES WADE
   10 ON ERROR PRINT TAB(0,0)"ERROR       RETYPE":GOTO 130
   20 MODE15:COLOUR 3
   30 DIM L%(511):start%=&1FD8000:finish%=&1FFFFFF:B%=4:O%=0
   40 CP%=&FF:R%=0:CK%=1:LS%=2:FSEL%=4:FS%=8:BLNK%=&20:WR%=&80
   50 PROCSETRD:PROCRESET:PROCUNBLANK
   60 DIM code%2000
   70 PROCassemble
   80 CLS:VDU28,65,31,75,0:CLS
   90 CALL scale
  100 LINE 1028,0,1028,1024:LINE1236,0,1236,1024:LINE1278,0,1278,1024
  110 REM Main programe loop START
  120 PRINT TAB(0,0) " READY     "
  130 IF INKEY(-114)=TRUE:SYS 6,147,&F1,&EF:WAIT:WAIT:SYS 6,147,&F1,&FF
  140 IF INKEY(-115)=TRUE:PROCSETRD:PROCRESET:CALL scale:CALL FStoCPU:
PROCLINE:PROCUNBLANK
  150 IF INKEY(-116)=TRUE:PROCINTDRAW
  160 IF INKEY(-21)=TRUE:PROCSTSTS
  170 IF INKEY(-117)=TRUE:PROCfilesave
  180 IF INKEY(-118)=TRUE:PROCfileload
  190 IF INKEY(-23)=TRUE:PROCLSCAN
  200 IF INKEY(-119)=TRUE:CALL GREY
  210 IF INKEY(-120)=TRUE:PROCECONST
  220 IF INKEY(-31)=TRUE:PROCDISPLAY2
  230 IF INKEY(-29)=TRUE:PROCSCREEN
  240 IF INKEY(-30)=TRUE: *HARDCOPYRX
  250 IF INKEY(-113)=TRUE:END
  251 *FX15
  260 GOTO 130:REM Main program loop END
  270 CLS:MOVE1024,0:DRAW1024,1024:MOVE1278,0:DRAW1278,1024:MOVE1236,0:
DRAW1236,1024
  280PROCSETRD:PROCRESET
  290 CALL code%
  300 PROCLINE:PROCUNBLANK
  310 REM*SAVE"PictureW/S" 1FD8000 1FFFFFF
  320 CALL GREY
  330 END
  331
  340 DEFPROCSETRD
  350  CP%=&FF-BLNK%:SYS "OS_Byte",147,&F1,CP%
  360  time%=TIME:REPEAT UNTIL TIME>time%+25
  370 ENDPROC
  371
  380 DEFPROCSETWR
  390  CP%=&FF-BLNK%-WR%:SYS "OS_Byte",147,&F1,CP%
  400  time%=TIME:REPEAT UNTIL TIME>time%+25
  410 ENDPROC
  411
  420 DEFPROCUNBLANK
  430  CP%=&FF-BLNK%:SYS "OS_Byte",147,&F1,CP%
  440  time%=TIME:REPEAT UNTIL TIME>time+25
  450  CP%=&FF:SYS "OS_Byte",147,&F1,CP%
  460 ENDPROC
  461
  470 DEFPROCCLOCK
  480  SYS 6,147,&F1,CP%-CK%:SYS 6,147,&F1,CP%
  490 ENDPROC
  491
  500 DEFPROCLINE
  510  SYS "OS_Byte",147,&F1,CP%-LS%:SYS "OS_Byte",147,&F1,CP%
```

Figure 3.6.1(a) CAIN SOFTWARE LISTING.

```
  520 ENDPROC
  521
  530 DEFPROCRESET
  540  SYS "OS_Byte",147,&F1,CP%-FS%:SYS "OS_Byte",147,&F1,CP%
  550  FOR N%=1 TO 30 :PROCLINE:NEXT
  560 ENDPROC
  561
  570 DEF PROCfilesave
  571  *FX15
  580  INPUT"File Save"''"Please"'"Enter"'"Filename"'FILE$
  590  CLS:OSCLI "SAVE" "+FILE$+" "+STR$~start%+" "+STR$~finish%
  600 ENDPROC
  601
  610 DEF PROCfileload
  620  INPUT"File Load"''"Please"'"Enter"'"Filename"'FILE$
  630  CLS:OSCLI "LOAD "+FILE$+" "+STR$~start%
  640 ENDPROC
  641
  650 DEF PROCassemble
  660  FOR pass%=0 TO 3 STEP 3:P%=code%
  670
  680  [ OPT pass%
  690 .scale STMFD R13!,{R0-R12,R14}
  700  MOV R4,£&1000000:ADD R4,R4,£&FD0000:ADD R4,R4,£&8000
  710  MOV R6,£20:MOV R7,£256:MOV R8,£640
  720 .loop MUL R3,R7,R8:ADD R3,R3,R4:SUB R3,R3,£2:SUB R7,R7,£1
  730 .loop2 STRB R7,[R3]:SUB R3,R3,£1:SUB R6,R6,£1:CMP R6,£0:BNE loop2:MOV
R6,£20:CMP R7,£0:BNE loop:LDMFD R13!,{R0-R12,PC}
  740 .FStoCPU STMFD R13!,{R0-R12,R14}:MOV R7,£&FF:MOV R4,£&1000000:ADD
R4,R4,£&FD0000:ADD R4,R4,£&8000
  750 .line MOV R0,£147:MOV R1,£&F1:MOV R2,£&DD:SWI 6:MOV R2,£&DF:SWI 6
  760  MOV R6,£&200:ADD R6,R6,£1:CMP R7,£0:BEQ line4:SUB R7,R7,£1
  770 .line2 SUB R6,R6,£1:CMP R6,£0:BEQ line3
  780  MOV R0,£146:MOV R1,£&F1:MOV R2,£0:SWI 6:STRB R2,[R4]
  790  MOV R0,£147:MOV R1,£&F1:MOV R2,£&DE:SWI 6
  800  ADD R4,R4,£1
  810  MOV R0,£147:MOV R1,£&F1:MOV R2,£&DF:SWI 6:B line2
  820 .line3 ADD R4,R4,£&80:B line
  830 .line4 LDMFD R13!,{R0-R12,PC}
  840;
  850 .GREY STMFD R13!,{R0-R12,R14}
  860  MOV R4,£&1F00000:ADD R4,R4,£&D8000:MOV R5,£&2000000
  870 .GREY2 LDRB R0,[R4]:MOV R0,R0,ROR £4:AND R2,R0,£&C
  880  CMP R2,£4:ADDEQ R0,R0,£40
  890  CMP R2,£8:ADDEQ R0,R0,£200
  900  CMP R2,£12:ADDEQ R0,R0,£240
  910  STRB R0,[R4]
  920  ADD R4,R4,£1:CMP R4,R5:BNE GREY2
  930  LDMFD R13!,{R0-R12,PC}
  940  ]:NEXT pass%
  950 ENDPROC
  960
  970 DEF PROCECONST
  980  REM This procedure is called ELLIPSE1 since in B+W it finds the
ellipse
  990  REM constants
 1000  M%=293:RATIO=1.42379148:H%=519:U%=457
 1010  PRINT TAB(0,0)"ELLIPSE1"
 1020  PROCEDRAW:REPEAT:PROCEDRAW:MOUSE H%,U%,BUTTON%:PROCEDRAW
 1030  IF BUTTON%=1:PROCEDRAW:M%=M%+1:PROCEDRAW
 1040  IF BUTTON%=2:PROCEDRAW;M%=M%-1:PROCEDRAW
 1050  IF INKEY(-26):PROCEDRAW:RATIO=RATIO/1.005:PRINT TAB(0,0) RATIO:
PROCEDRAW
```

Figure 3.6.1(b) CAIN SOFTWARE LISTING.

```
 1060  IF INKEY(-122):PROCEDRAW:RATIO=RATIO*1.005:PRINT TAB(0,0) RATIO:
PROCEDRAW
 1070  UNTIL INKEY(-74):PROCEDRAW:PRINT H%;",";U%
 1080  REM ellipse centred at graphic co-ordinates H% and U%
 1090  REM the values to be returned to MAIN PROG
 1100  REM are H%,U%,M%,RATIO
 1110 ENDPROC
 1120
 1130 DEF PROCEDRAW
 1140  REM this draws an ellipse using the ELLIPSE command
 1150  GCOL 4,0:ELLIPSE H%,U%,M%,RATIO*M%
 1160  MOVE H%-100,U%:PLOT 6,H%+100,U%:MOVE H%,U%-100:PLOT 6,H%,U%+100
 1170 ENDPROC
 1180
 1190 DEF PROCINTDRAW
 1200  MODE15:VDU 28,65,31,75,0:LOCAL V%(),W%(),S%:DIM V%(1000),W%(1000)
 1210  PRINT TAB(0,0)"INTDRAW":S%=0:A%=M%:FILE=OPENIN "TESTDATA"
 1220  REPEAT
 1230  INPUT£ FILE,V%(A%),W%(A%):A%=A%+1
 1240  UNTIL EOF£ FILE:CLOSE£ FILE
 1250  PROCRDRAW
 1260  REPEAT
 1270  IF INKEY(-122)CLG::S%=S%+1:PROCRDRAW:PRINT TAB(0,0)S%
 1280  IF INKEY(-26)CLG:S%=S%-1:PROCRDRAW:PRINT TAB(0,0)S%
 1290  UNTIL INKEY(-99):PRINT TAB(0,0)" READY   "
 1300 ENDPROC
 1310
 1320 DEF PROCSTATS
 1330  PRINT "STATISTICS"
 1340  LOCAL ST%(),FMAX%:DIM ST%(255):FMAX%=0
 1350  FOR I%=&1FD8000TO&1FFFFFF:ST%(?I%)=ST%(?I%)+1:NEXT
 1360  FOR I%=2TO255STEP2:IF ST%(I%)>FMAX% FMAX%=ST%(I%):M%=I%
 1370  NEXT:MODE15:MOVE 1020,100:DRAW 0,100:DRAW 0,600:MOVE 8,100:GCOL 0,14
 1380  COLOUR 100:FOR I%=2TO255STEP2:DRAW I%*4,100+ST%(I%)*500/FMAX%:NEXT
 1390  PRINT TAB(0,30) "0":PRINT TAB(42,30)"Intensity --->     255"
 1400  PRINT TAB(0,12)"Frequency":VDU28,65,31,75,0
 1410 ENDPROC
 1420
 1430 DEF PROCLSCAN
 1440  PRINT TAB(0,0) "LINESCAN":IF Y%<10 Y%=128
 1450  PROCINVERT
 1460  REPEAT
 1470  IF INKEY(-42) PROCUNINVERT:Y%=Y%+1:PROCINVERT
 1480  IF INKEY(-58) PROCUNINVERT:Y%=Y%-1:PROCINVERT
 1490  UNTIL INKEY(-99)
 1500  PROCUNINVERT
 1510  PROCSAMPLE
 1520  PROCDISPLAY
 1530  REPEAT UNTIL INKEY(-99)
 1540  PROCDISPLAY:PRINT TAB(0,0) " READY  "
 1550 ENDPROC
 1560
 1570 DEF PROCUNINVERT
 1580  S%=Y%*640+&1FD8000
 1590  FOR N%=0TO511:?(N%+S%)=?(N%+S%)-100:NEXT
 1600 ENDPROC
 1610
 1620 DEF PROCDISPLAY
 1621  PRINT TAB(0,0)"MAGN = ";B%/4
 1630  MOVE 0,L%(0):FOR N%=0TO511:PLOT 6,N%*2,B%*L%(N%)+O%:NEXT
 1640 ENDPROC
 1650
 1660 DEF PROCDISPLAY2
```

Figure 3.6.1(c) CAIN SOFTWARE LISTING.

```
1670  CLG:GCOL 25:MOVE 1024,0:DRAW 0,0:DRAW 0,1024:GCOL 50:PROCDISPLAY
1680  REPEAT:IF INKEY(-58) PROCDISPLAY:B%=B%+1:PROCDISPLAY
1681  IF INKEY(-42) PROCDISPLAY:B%=B%-1:PROCDISPLAY
1682  IF INKEY(-122) PROCDISPLAY:O%=O%+50:PROCDISPLAY
1683  IF INKEY(-26) PROCDISPLAY:O%=O%-50:PROCDISPLAY
1684  UNTIL INKEY(-99)
1690 ENDPROC
1700
1710 DEF PROCINVERT
1720  S%=Y%*640+&1FD8000
1730  FOR N%=0TO511:?(N%+S%)=?(N%+S%)+100:NEXT
1740 ENDPROC
1750
1760 DEF PROCSAMPLE
1770  LOCAL C%:FOR N%=0TO511:L%(N%)=0:NEXT:FOR C%=Y%TOY%+4
1780  S%=C%*640+&1FD8000
1790  FOR N%=0TO511:L%(N%)=L%(N%)+?(N%+S%):NEXT:NEXT
1800  FOR N%=0TO511:L%(N%)=L%(N%)*0.2:NEXT
1810 ENDPROC
1820
1830 DEF PROCSCREEN
1840  REM ELLIPSE 1 passes the variables H%,U%,M%,RATIO
1850  REM X%,Y% starting co-ords, M% the minor axes length,RATIO
1860  LOCAL V%(),W%(),NV%(),NW%(),MAJ,MIN,SX%,SY%
1870  DIM V%(1000),W%(1000),NV%(1000),NW%(1000)
1880  SX%=H%*0.5:SY%=255.75-U%*0.25
1890  FOR R%=20TOM%
1900  MIN=R%*0.5:MAJ=MIN*RATIO*0.5
1910  FOR X%=SX%TOSX%+MIN
1920  S%=MAJ*SQR(1-((X%-SX%)/MIN)^2)
1930  Y%=SY%+S%:IF ?(&1FD8000+640*Y%+X%)=255 GOTO 1990
1940  V%(R%)=?(&1FD8000+640*Y%+X%)+V%(R%):NV%(R%)=NV%(R%)+1
1950  ?(&1FD8000+640*Y%+X%)=255
1960  Y%=SY%-S%:IF ?(&1FD8000+640*Y%+X%)=255 GOTO 1990
1970  W%(R%)=?(&1FD8000+640*Y%+X%)+W%(R%):NW%(R%)=NW%(R%)+1
1980  ?(&1FD8000+640*Y%+X%)=255
1990  NEXT:NEXT
2000  FILE=OPENOUT "TESTDATA"
2010  FOR I%=10TOM%
2020  IF NV%(I%)=0 GOTO 2050
2030  IF NW%(I%)=0 GOTO 2050
2040  PRINT£ FILE, V%(I%)/NV%(I%),W%(I%)/NW%(I%)
2050  NEXT
2060  CLOSE£ FILE
2070 ENDPROC
2080
2090 DEF PROCRDRAW
2100  MOVE 2*M%,4*V%(M%):FOR I%=M%TOA%:DRAW 2*I%,4*V%(I%):NEXT
2110  MOVE 2*M%,4*W%(M%+S%):FOR I%=M%TOA%:DRAW 2*I%,4*W%(I%+S%)+200:NEXT
2120  MOVE 2*M%,2*(V%(M%)+W%(M%+S%))+400
2130  FOR I%=M%TOA%:DRAW 2*I%,2*(V%(I%)+W%(I%+S%))+400:NEXT
2140 ENDPROC
```

Figure 3.6.1(d) CAIN SOFTWARE LISTING.

Function key	Task description	Associated procedures
F1	Resets framestore to capture next triggered frame (trigger normally obtained from Nd:YAG laser)	———
F2	Samples current stored frame	SETRD,RESET, SCALE FS to CPU, LINE, code% UNBLANK
F3	Draws intensity/position of current picture	INTDRAW, RDRAW
F4	Draws histogram of the frequency of occurrence of intensity for current picture (to help obtain maximum dynamic range of camera/framestore)	STATS
F5	Saves the current picture to floppy disk (requires 160 kB memory)	FILESAVE
F6	Loads a picture from disk and displays on screen	FILELOAD
F7	Positions and samples intensity/position from 5 adjacent lines on screen	LSCAN, INVERT, SAMPLE, DISPLAY, UNINVERT
F8	Converts current colour picture to 16 level black and white picture with linear grey scale	GREY
F9	Displays ellipse on screen in order to allow user to find centre and equation of elliptical fringes produced by CAIN	ECONST, EDRAW
F10	Similar to F3 (except for expansion of y axis)	DISPLAY2,DISPLAY
F11	Activates elliptical averaging routine	SCREEN
F12	Activates screen–dump of current screen	———

Figure 3.6.2. Function Key Operation.

3.7 RESULTS

The interferometer was used to determine the beam-profile of the ND:YAG pump laser beam which was operated on a single longitudinal mode with a 10nS pulse duration.

Figure 3.7.2 is a photograph taken from a video monitor connected to the video output from the frame grabber of freeze frame mode. The picture shows the interference pattern of two pumped laser beams and the modulation pulses can be clearly seen. The modulation is of a 50 ps duration beam that was superimposed onto a pulse of longer duration.

Figure 3.7.1 shows five line computer averaging of a beam profile and was output onto a dot-matrix printer.

3.8 CONCLUSION

The objectives have been met and the system has been used for several experiments, the results of which have been verified with a streak camera. The computer has proved sufficient in speed and performance for the data analysis required.

Future improvements to the system would be to synchronise the CCD camera pixels to the video frame store which would improve the overall resolution of the system.

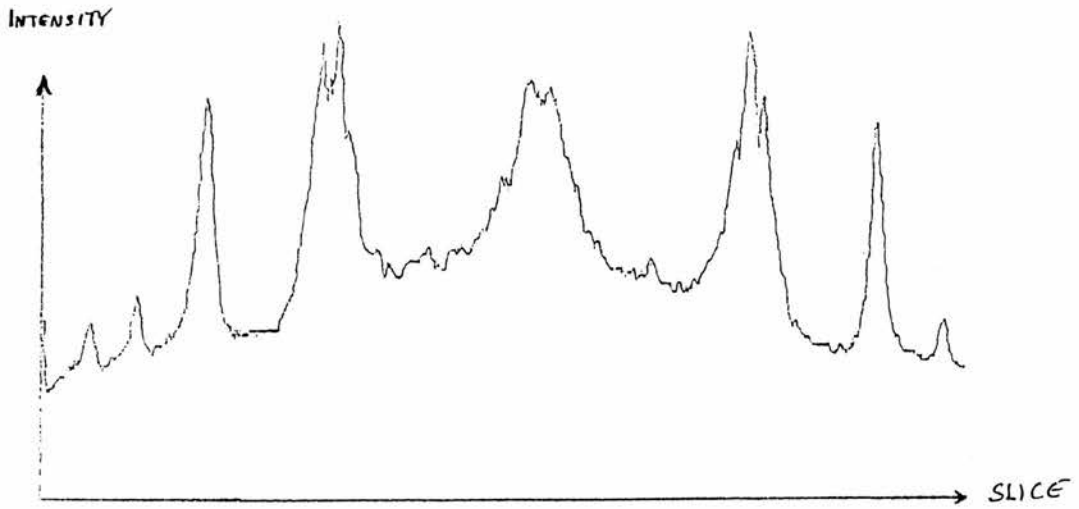

Figure 3.7.1. CAIN Five line average.

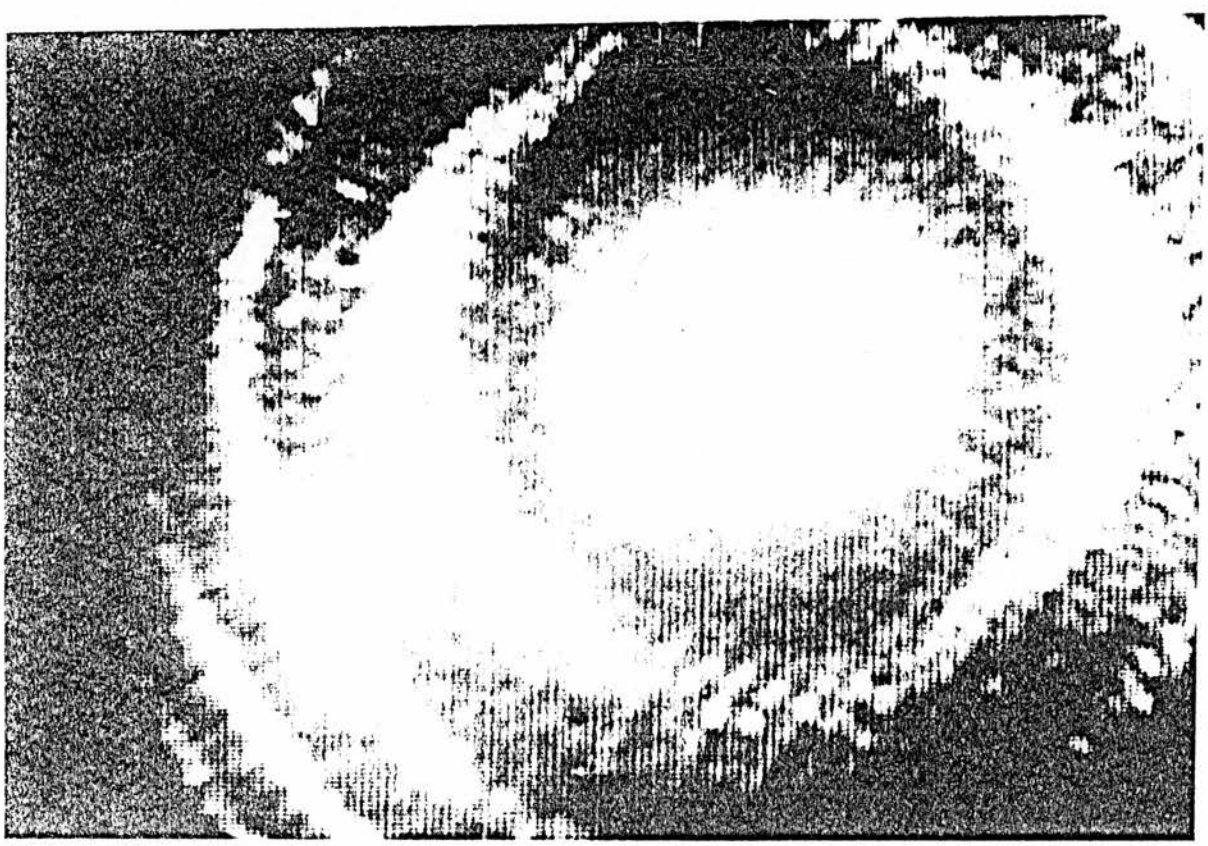

Figure 3.7.2. Beam Profile Interferogram.

3.9 BIBLIOGRAPHY

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CHAPTER 4

1728 BIT LINEAR CCD CAMERA

CHAPTER 4 1728 BIT LINEAR CCD CAMERA

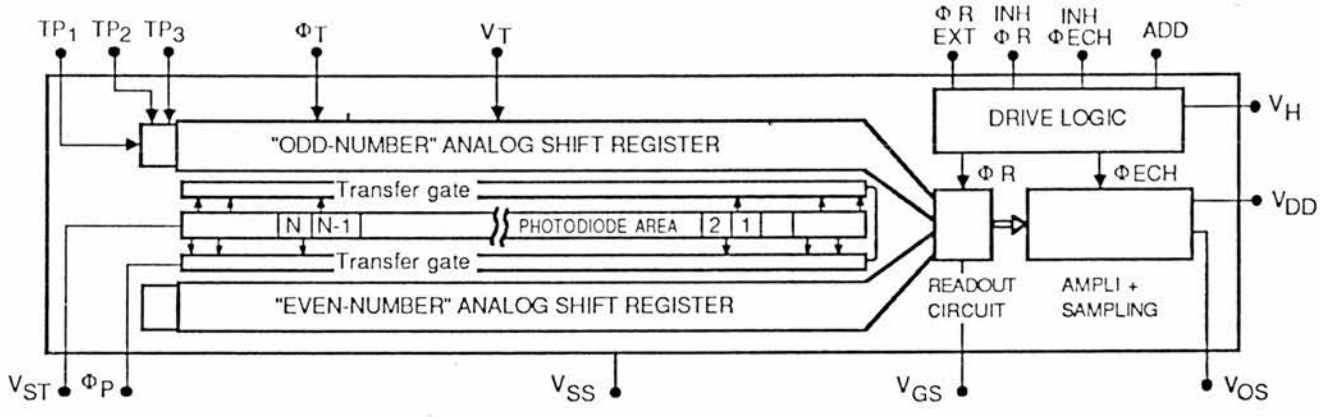
4.1 INTRODUCTION

The linear CCD camera is a very compact high resolution linear array CCD optical sensing camera, containing an on board 12 bit analogue to digital convertor with a high speed fibreoptic data link. The camera was designed using surface mount technology resulting in its compact size. The complete circuit is contained in a miniature flanged die-cast box measuring only 28mm * 34mm * 88mm. As a direct result of the camera being compact and totally screened, the camera can operate in harsh electrical environments such as being connected to the live chassis of a high power pulsed laser. Furthermore microcomputer switching noise and earth loops are eliminated by way of the fibreoptic link.

4.2 CCD DESCRIPTION

The CCD used is a Thomson-CSF TH 7801 solid-state image sensor composed of a linear array of 1728 photodiodes. Each photodiode measures 13um * 13um, with 13um centre-to-centre spacing. The useful length of the photosensitive area is 22.464 mm.

The CCD construction is shown in figure 4.2.1



Φ = Phase

Figure 4.2.1. TH7801 CCD Block Schematic.

Each image-sensor is made up of a n-p photodiode, overlaid with silicon and associated with a storage capacitor that collects the electrons created by incident light. The quantity of stored charge is directly proportional to the illumination and integration (exposure

time). This structure provides high sensitivity, because it avoids the problem of incident-light absorption by the electrodes, such as encountered with a photo-MOS structure, for example.

At each end of the linear array, four masked elements provide a "dark signal" reference level. An internal transfer gate isolates the photosensitive array from the shift registers, by means of a potential barrier. The opening of this barrier allows the parallel transfer of the charges accumulated in the photosensitive zone by way of control "phase T", a transfer occurs on each toggle of this logic input.

TWO CCD ANALOGUE SHIFT REGISTERS

2 CCD analogue shift registers are situated one on each side of the linear array. One of these receives the charges generated by "even-numbered" photosensitive elements, the other from charges generated by "odd-number" elements. These registers sequentially transfer the charges issuing from each photoelement towards the output circuit. Parallel to these shift registers are two supplementary registers (one on each side), which insulate them from the periphery of the circuit and suppress the peripheral dark current and electrode noise.

OUTPUT CIRCUIT

The charges issuing from each shift register are multiplexed in a common detector diode, which converts them into a voltage. Between each arrival of a charge packet, the

detector-diode potential is fixed at a reference level by a preloading MOS transistor.

The detector diodes potential is applied to the input of an amplifier, which delivers a sample-and-hold video output signal. This output is under low impedance and proportional to the light incident on the line to be analyzed.

INTEGRATED DRIVE ELECTRONICS

An internal logic circuit generates the reset clock signal for the detector diode "phase R" and for the sample clock "phase ech". This internal circuit reduces the number of external clock signals necessary to only two (output transfer clock "phase T" and internal transfer clock "phase P"). Their timing relationship and corresponding video output is shown in figure 4.2.2.

INTEGRATION TIME CONTROL

The transfer clock phase "P" makes it possible to control the light integration (exposure) time of the photo elements. The integration time is the time interval between two successive trailing edges of "phase P".

OUTPUT DATA RATE CONTROL

The readout clock, "phase T", controls the data rate of the video line. The output data rate is twice the frequency of "phase T", that is, data is output on rising and falling edges of this phase input.

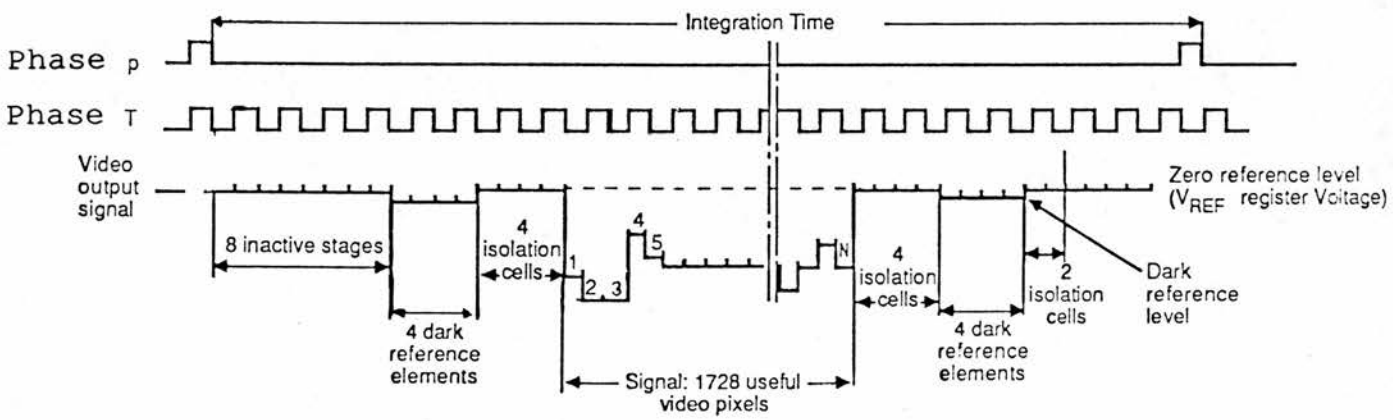


Figure 4.2.2. TH7801 Video output line.

4.3. CIRCUIT DESCRIPTION

The circuit descriptions are made with reference to the 6 circuit diagrams and component list which are located at the end of this chapter.

Figure 4.3.4 SCHEMATIC.

Figure 4.3.5 CCD.

Figure 4.3.6 ANALOGUE PROCESSING.

Figure 4.3.7 ADC.

Figure 4.3.8 CONTROL / OUTPUT REGISTER.

Figure 4.3.9 POWER SUPPLY.

Figure 4.3.10A/B COMPONENT LIST.

4.3.1 CONTROL TIMING.

After switch-on the first video line output will be false data and should be ignored until the second readout sequence is initiated. This is due to the integration effect of the CCD and thus the first video line output will be saturated. The description to follow is assuming that after switch-on the first video line has been clocked out.

To start a new frame, counter U10 must first be reset and this is accomplished by applying a logic "Low" on the "CLK" clock line for a preset time interval, allowing C10 to be discharged through R20 and the slowly changing waveform is cleaned up by Schmitt trigger U12C. Its output will then go to logic "High", resetting counters U10A and U10B. The output of U12C also drives CCD phase "P" (figure 4.3.1) via U12D and U6A. Phase "P" is at logic "High" when in this reset mode. Applying this logic "High" informs the CCD to

start a new frame. The clock "CLK" line may now be brought to a logic "High" while allowing the capacitor resistor network to charge again, reversing the process, removing the reset signal. This capacitor resistor network is effectively a low pass filter, with normal clock pulses being too fast to be fed through the filter. This network may be considered as a selective switch activated by a time delay. The active "High" on the reset line of counter U10 has been removed, allowing this counter to be incremented. The CCD phase "P" is now logic "Low" figure 4.3.1 and the CCD transfers the linear array video line onto the CCD shift registers ready to be clocked out.

A monostable multivibrator is constructed from quad NAND gate U11. The inputs to U11B are fed from the same signal source except one side is connected through three NAND gates connected up as invertors. The invertors delay the input signal by approximately 20nS. If a logic "High" to logic "Low" transition occurs on the input then the output will not change as the delayed input to U11B was already false and the direct input is now instantly false. The output will stay false and logic "High". If the input now goes now to logic "High", the direct input will be true and the delayed input will also be true for 20ns and a pulse will appear at the output for the same duration.

8 clock pulses are now applied to the camera and counter IC10A bit 3 (QD) will toggle to logic "High" and initiates the ADC to start conversion figure 4.3.2. IC11 monostable will now produce a pulse on this rising edge from IC10A bit 3 and its output is fed to the load input of the

shift registers with the last ADC data now being latched. Now that the ADC has been requested to start conversion, the "BUSY" output goes active "Low" until the conversion is complete with the application of clock pulses.

12 clock pulses are now applied and at the end of which the "Busy" output from the ADC goes inactive "High" (figure 4.3.2) and is used to drive invertor U12F and onto the clock input of counter U10B which toggles its least significant bit. This counter output is used to drive CCD phase "T" via buffer U6B. Phase "T" shifts out the next video pixel from the CCD.

4 clock cycles later and this interval has neatly solved a few timing problems in that it has allowed the propagation delays inherent in the analogue electronics from the CCD through to the ADC and allows the analogue signal to settle at the ADC input, as can be seen from "TD" from figure 4.3.2. It should be noted that the output from the CCD is a sample-and-hold signal and thus remains constant between update requests. This is necessary as the analogue input to the ADC must remain constant over its entire conversion cycle. At the same time the load input of the shift register is pulsed by monostable IC11 to latch the last ADC sample, also the ADC is requested to start conversion of the latest video pixel from counter U10A, repeating the whole process.

This entire sequence continues until all 1728 pixels plus reference pixels are read out before a new frame is initiated with the reset sequence. The time duration between cycles is the integration (exposure) time of the CCD.

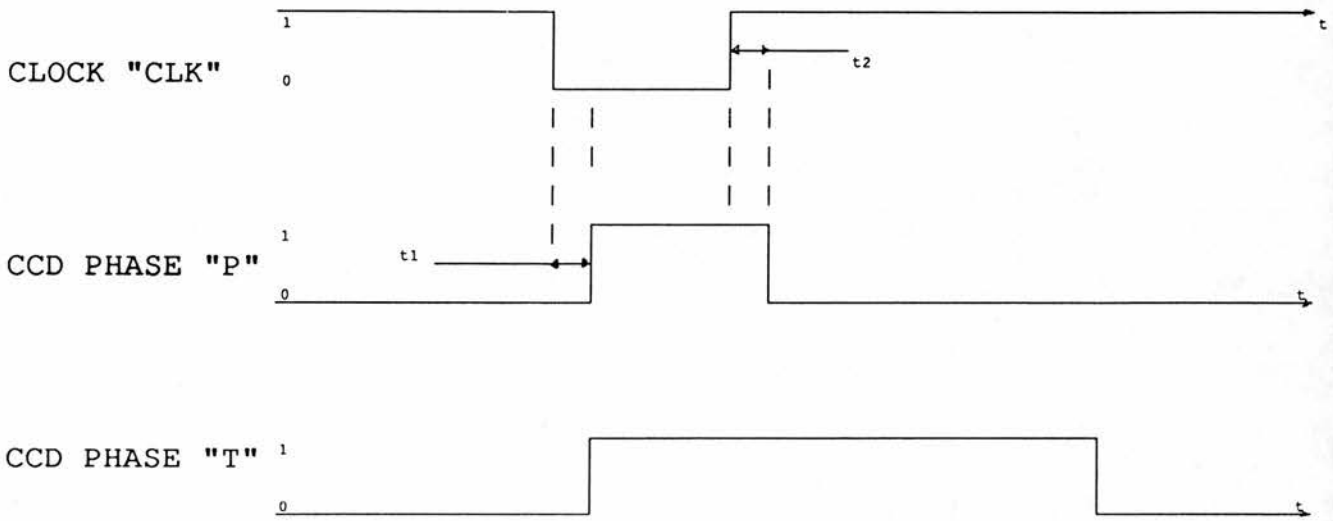


Figure 4.3.1. FIELD-START TIMING DIAGRAM

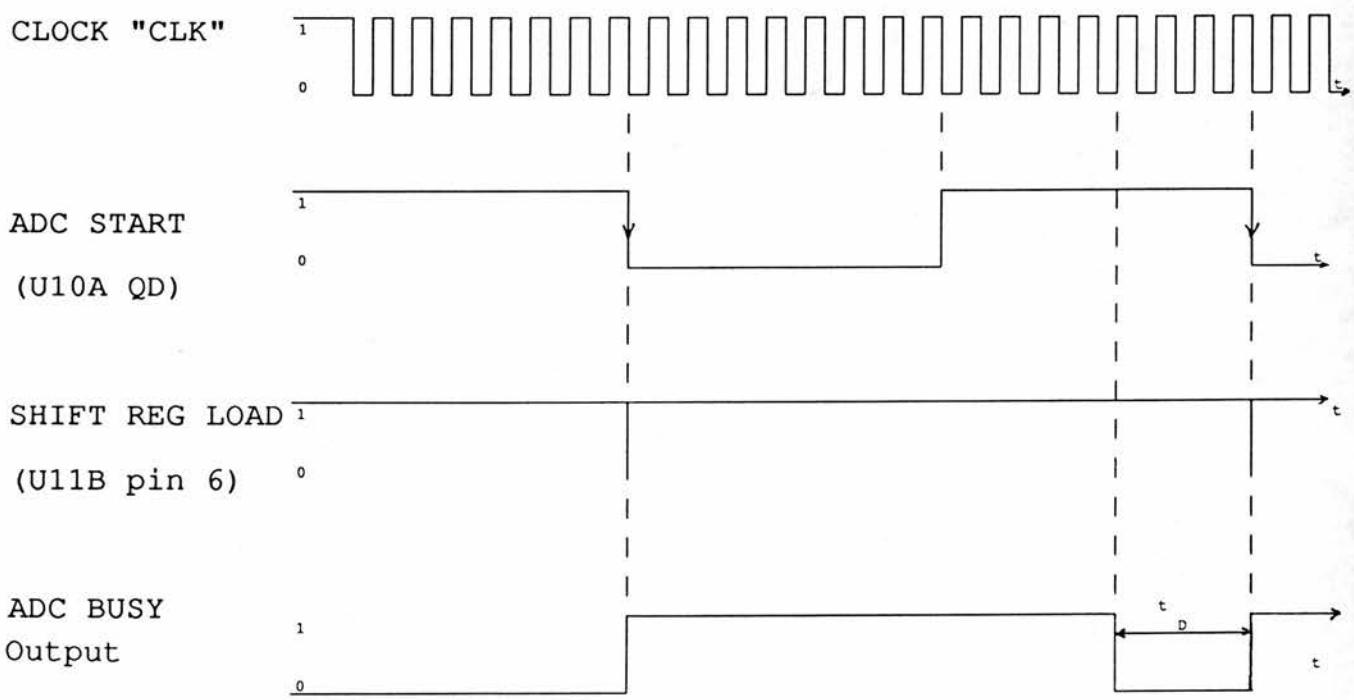


Figure 4.3.2 ADC TIMING DIAGRAM

4.3.2 SHIFT REGISTER TIMING.

The shift register circuit description is made with reference to figure 4.3.8 control / output register circuit diagram.

A 12 bit shift register is constructed from two 8 bit devices (U8 and U9) and are connected in series. Unused inputs are connected to QH output pin on U9 due to PCB space restrictions and all CMOS input pins must be connected to either logic "High" or "Low" to prevent latchup. New data is presented to the shift register every 16 clock cycles and latched in on the "CLK" clock falling edge. The shift register shifts data out on a rising edge thus timing continuity is maintained. Thus on the first clock cycle data is read in on the falling edge and output on the rising edge.

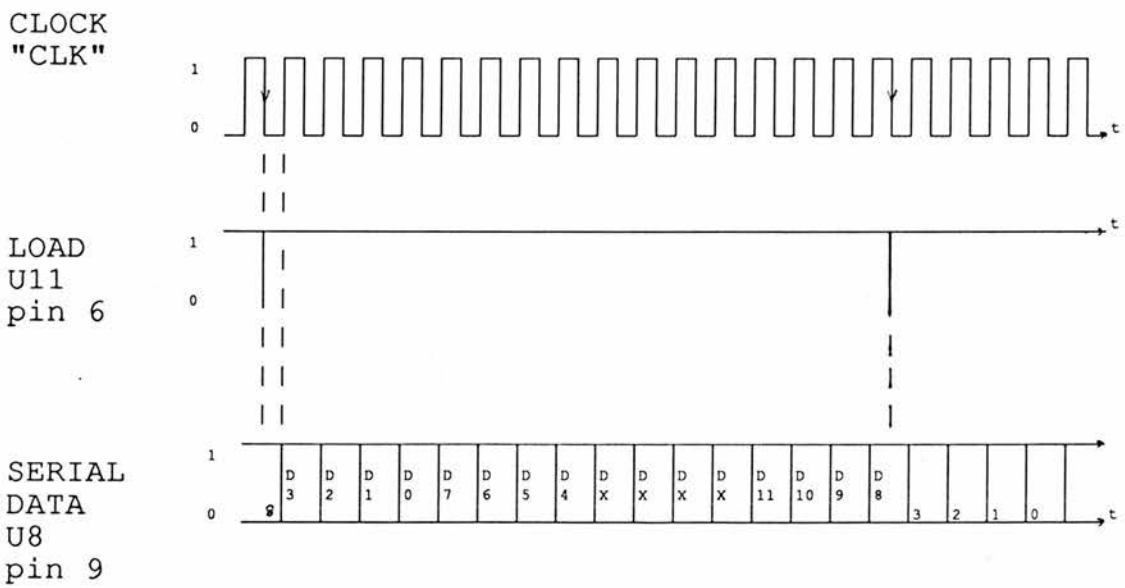


Figure 4.3.3 SERIAL DATA TIMING DIAGRAM

4.3.3 CCD CONNECTION

The phase input logic driving requirements for the CCD are +12V +/- 1 volt for logic "High" and 0 to 0.6 volts for logic "Low" and thus cannot be directly driven from TTL. MOS CLOCK driver U6A and U6B, a dual DS0026 National semiconductors device, provides the high voltage and the fast rise and fall times necessary to drive the CCD phases. Current limiting resistors are used between their outputs and the CCD to help reduce signal noise on the analogue output waveform from the fast rise times of the driver.

There are only 2 power supply requirements for the CCD, one for the analogue and one for the digital. The analogue supply is +6.3V and the logic supply is +13.5V, decoupled and filtered by C12, C13 and L1.

The analogue output comes from pin 21, which is fed to the analogue processing conditioning amplifiers.

4.3.4 ANALOGUE PROCESSING.

The analogue video frame from the CCD is referenced to +6.3 volts and grows downwards with applied intensity. The requirement for the ADC is that it should be referenced to ground and grow upwards with intensity, reaching full scale just before saturation is met.

U2 quad operational amplifier is a high slew rate high input impedance component. Differential amplifier U2D is connected to remove the DC bias with the 6.3 volt line connected to the non-inverting input and thus rejects the DC bias leaving the analogue waveform referenced to ground,

being also inverted to the required configuration. The output is then applied across a potential divider that allows the output to be calibrated for full-scale when a near saturated CCD light intensity is applied to the CCD.

U2C and U2B amplify the video by a factor of 4, the output is connected directly to the analogue input of the ADC.

4.3.5 ANALOGUE TO DIGITAL CONVERTER

The ADC used is an Analog Devices type AD7672 high speed 12 bit converter, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC^2MOS) process, which combines precision bipolar components with low power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparitor in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3uS while dissipating only 110mW of power.

The analogue input to the ADC can be unipolar or bipolar with a 5 volt or 10 volt span. The video input is from 0 to 5 volts so the unipolar 5 volt input configuration is used. The supply voltage requirements are +5V for VDD, -5V reference and -12.5 volts. All these voltages are generated from the power supply apart from the -12 volt line, this being derived from the -13.5 volt line with two forward biased diodes to generate a voltage drop, reducing the supply voltage to the required level. Two capacitors are used to decouple this supply line to prevent unwanted oscillation.

The system clock is derived from the CLK output of the ADC with the fibre optic receiver's output feeding the clock input of the ADC. The conversion time is thus governed by the input clock. The maximum conversion time of the convertor is 3uS added to the 4 redundant clock cycles for analogue processing and the conversion time for one pixel takes 4uS. The clock frequency is 16 times this value and is 4MHz.

4.3.6 FIBRE OPTIC DATA LINK

The fibre optic data-link uses state of the art self contained modules for the transmitter and receiver. The receiver module features a shielded integrated photodetector and wide bandwidth DC amplifier for high EMI immunity. A Schottky clamped open-collector output transistor allows direct interfacing to common logic families. The typical baud rate of this device is 5M bits s^{-1}.

The transmitter module utilizes an IR light emitting diode with a maximum bit rate of 5M bits s^{-1} with a forward current of 60 mA. The driver circuitry uses a MOSFET transistor Q1 to deliver the required drive current of 60 mA via the current limiting resistor R22. The gate input to Q1 is TTL compatible and is directly driven by the logic.

The maximum distance in which the link will operate over the temperature range 0 to 70 degrees C is 17 metres using standard polymer cable that is terminated just with a sharp knife at 90 degrees at each end.

4.3.7 POWER SUPPLY

The power supply derives five output voltages from a single unregulated DC input of +15 V (+14.5 to +25V). The +5 volt rail is derived from a fixed +5V 100mA regulator U6. The +13.5 volt regulation is derived from a fixed +5V regulator with its ground pin connected to ground with a +8.2 volt Zener diode thus raising its reference point to give the required output voltage. The four large value capacitors connected between ground and the regulators 0V pin and between its output and its 0V pin prevent the regulator from bursting into oscillation.

A DC to DC hybrid convertor is used to generate the -13.5V rail and this will mirror the input voltage to an exact negative one and is connected to the +13.5V line.

The -5V reference is generated from a precision Zener diode and only requires the addition of a current limiting resistor and decoupling capacitor to generate a highly stable reference voltage.

The +6.3 volt line is generated with an operational amplifier connected in the inverting mode with a gain of 1.25 with its input connected to the -5V reference. It should be noted that the CCD output waveform is generated from the +6.3 volt line and variations in this is shown at the CCD's analogue output. The analogue to digital convertor uses the -5V rail as its reference. If the -5V rail changes so will the 6.3V rail and is thus self tracking which makes for a very stable circuit.

4.4 TEST DECODER DRIVER

The Test Decoder Driver circuit uses a standard oscilloscope to display the digital bit pattern of the camera output, which illustrates the background light level as opposed to individual pixel performance. The circuit is used to stimulate the CCD camera's circuitry in every respect.

The basic schematic concept may be used to build a Microcomputer-add-on-card that could store multiple video lines and enable the integration and sample times to be variable to enable the CCD camera to be utilized to its fullest potential depending on the specific application. The fact that the interface will be contained in a noisy switching environment within the computer is not a problem because the decoder is all digital and isolated from the camera by the fibre-optic data link.

CIRCUIT DESCRIPTION

The complete decoder is shown in block form in figure 4.4.1 and the complete circuit diagram in figure 4.4.3 with the timing diagram in figure 4.4.2 with the time critical frame transfer of the camera also outlined.

The "Master Clock" is derived from an external TTL pulse generator set-up for the cameras maximum pulse repetition rate of 4MHz. This clock is used to feed the divider and the AND gate.

The "Divider" has two outputs one at 2^8 and the other at 2^{14}. The first triggers the oscilloscope at the start of a new pixel and the second indicates the end of a complete

video line output. The "Divider" has a reset input which is used to clear the divider outputs to logic "Low" at the end of each video line transfer ready for the start of a new video line.

Monostable multivibrator "A" generates a pulse at the start of a new video line so that the camera can initiate a frame transfer. The pulse delay should be made long enough to allow the low pass filter in the camera to go active. Once the low pass filter's output is set then sufficient time must be allowed to let the filter discharge again before clock pulses are applied to read out the first pixel and monostable multivibrator "B" is used to set this delay and its minimum delay time is twice the delay of "A". The maximum delay time of monostable "B" is set with "VR1" variable resistor which determines the integration time of the camera. The "D" register (U7) on the output of monostable "B" synchronises its output with the clock after a reset sequence and prevents jitter.

The output stage uses a TTL compatible MOSFET driver transistor to drive the fiberoptic transmitter. The fiberoptic receiver is connected directly to the oscilloscope for monitoring. The oscilloscope should be set to show 16 bits, which is the data length of each pixel.

CIRCUIT EXPANSION

To extend the test circuit into a computer interface is fairly straight forward. The interface would include a temporary memory store, a 8 bit tri-state shift register to store one pixel into two memory locations. The address for

the tempoary store would be taken from the "divider". The computer interface would be able to read the memory with a tri-state buffers. The "master clock" would need to be driven from the computer to allow memory locations to be rippled through at leisure. Sequential logic would be used to read in two complete lines of video to set-up the integration time and then freeze the last frame onto memory. The complete circuit would fit easily onto a plug-in card for a microcomputer.

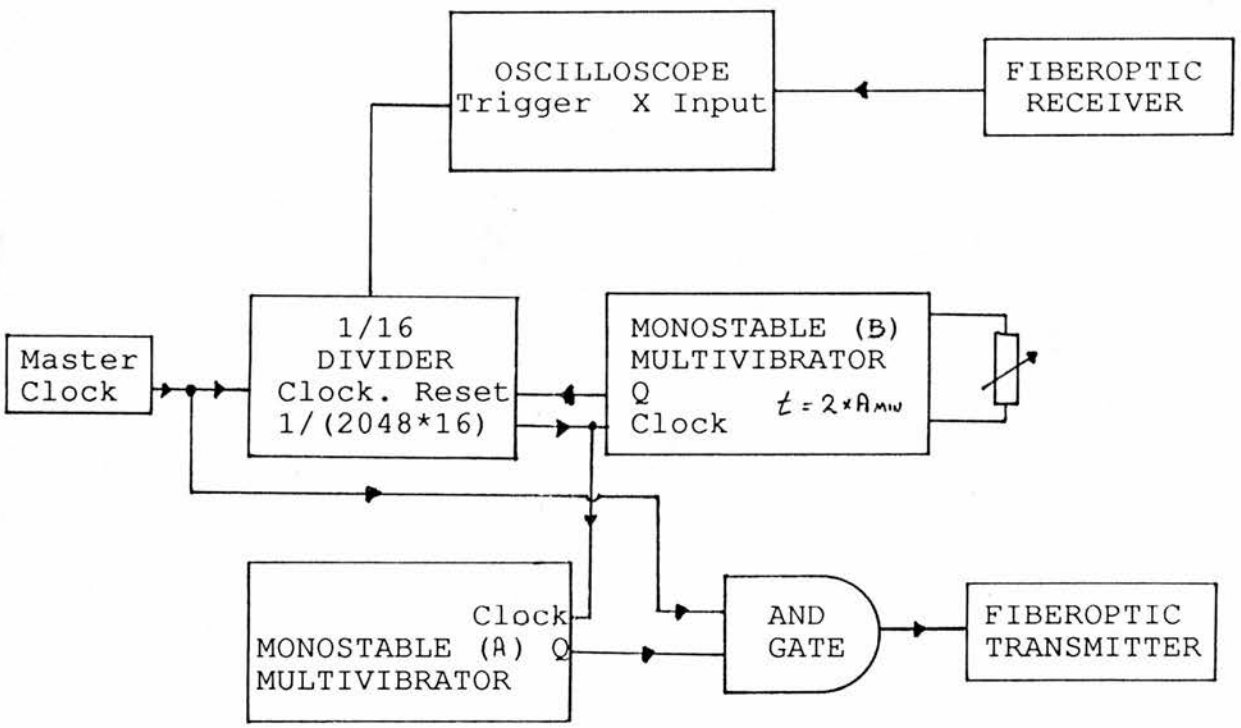


Figure 4.4.1. Test decoder driver block schematic

4.5 CONCLUSION

From monitoring the analogue output of the CCD the quality and stability appear to be laboratory standard, although it will not be proved until a computer interface has been implemented to fully verify the quality.

Future improvements would be to include a memory directly on to the 'Head' eliminating the need for a high speed data link. Also required would be an optical input for external triggering. The development for a decoder for the existing 'Head' might be for a stand alone unit with a serial data port that would enable the Head to be controlled from any computer with a serial communications channel. Multiple memory could be used to allow faster integration times to be achieved from The 'Head' to allow for the slow serial communications used.

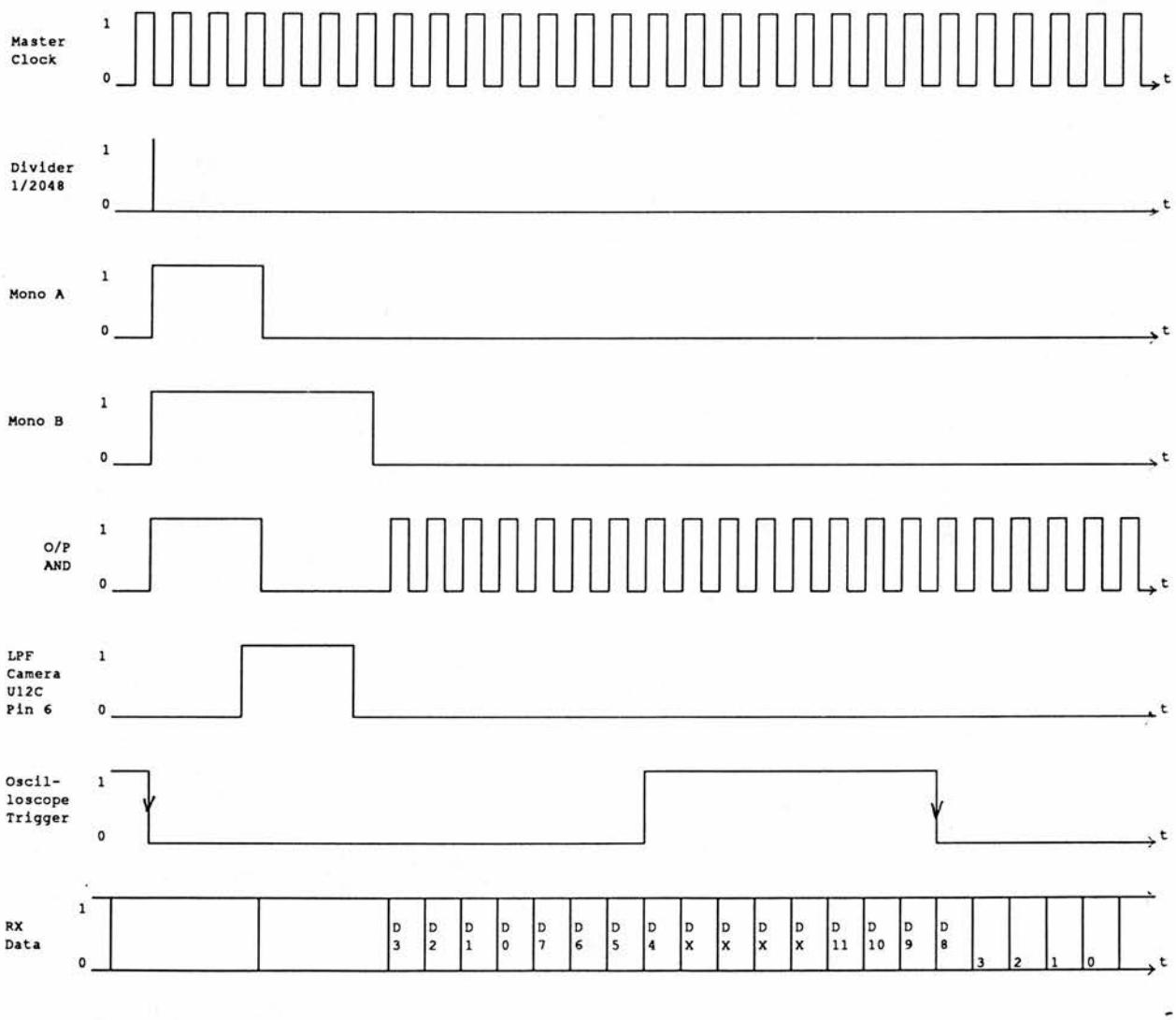


Figure 4.4.2. Test Decoder Driver Timing Diagram.

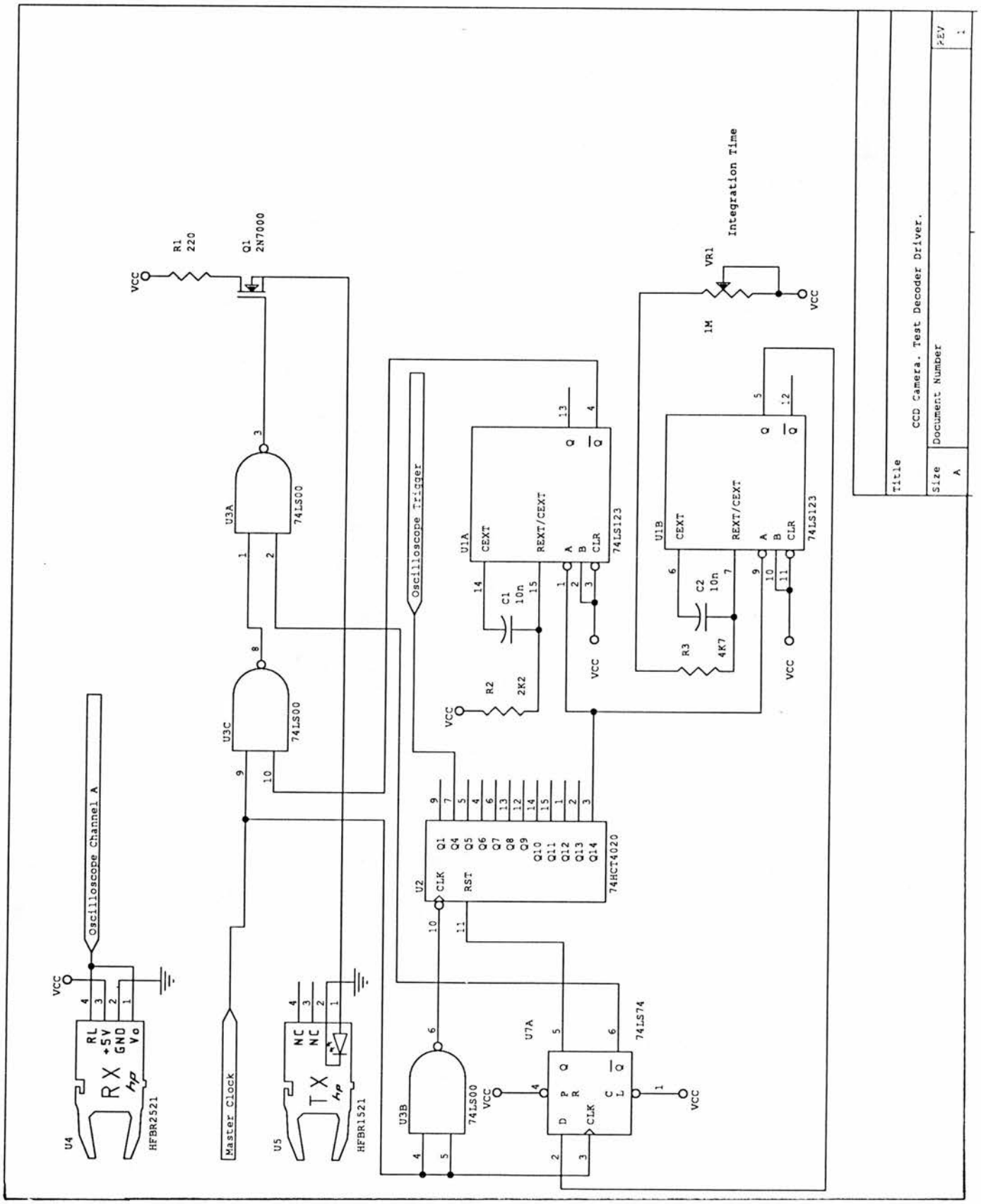


Figure 4.4.2. Test Decoder Driver Circuit Diagram

Test Decoder Driver component list.

Item	Quantity	Reference	Part
1	2	C1,C2	10n
2	1	Q1	2N7000
3	1	R1	220
4	1	R2	2K2
5	1	R3	4K7
6	1	U1	74LS123
7	1	U2	74HCT4020
8	1	U3	74LS00
9	1	U4	HFBR2521
10	1	U5	HFBR1521
11	1	U7	74LS74
12	1	VR1	1M

Figure 4.4.4. Test Decoder Driver Component list.

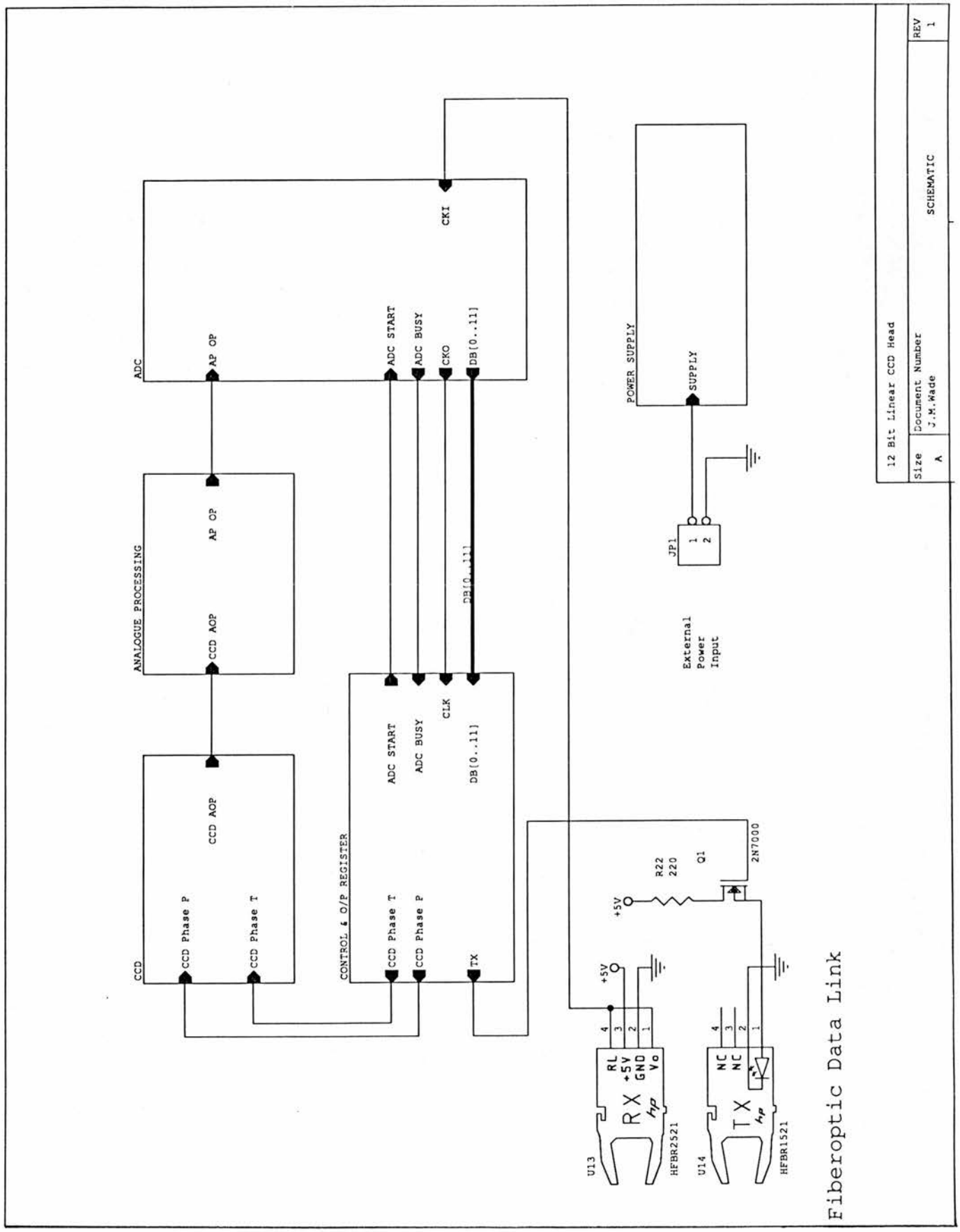


Figure 4.3.4. Schematic Circuit diagram.

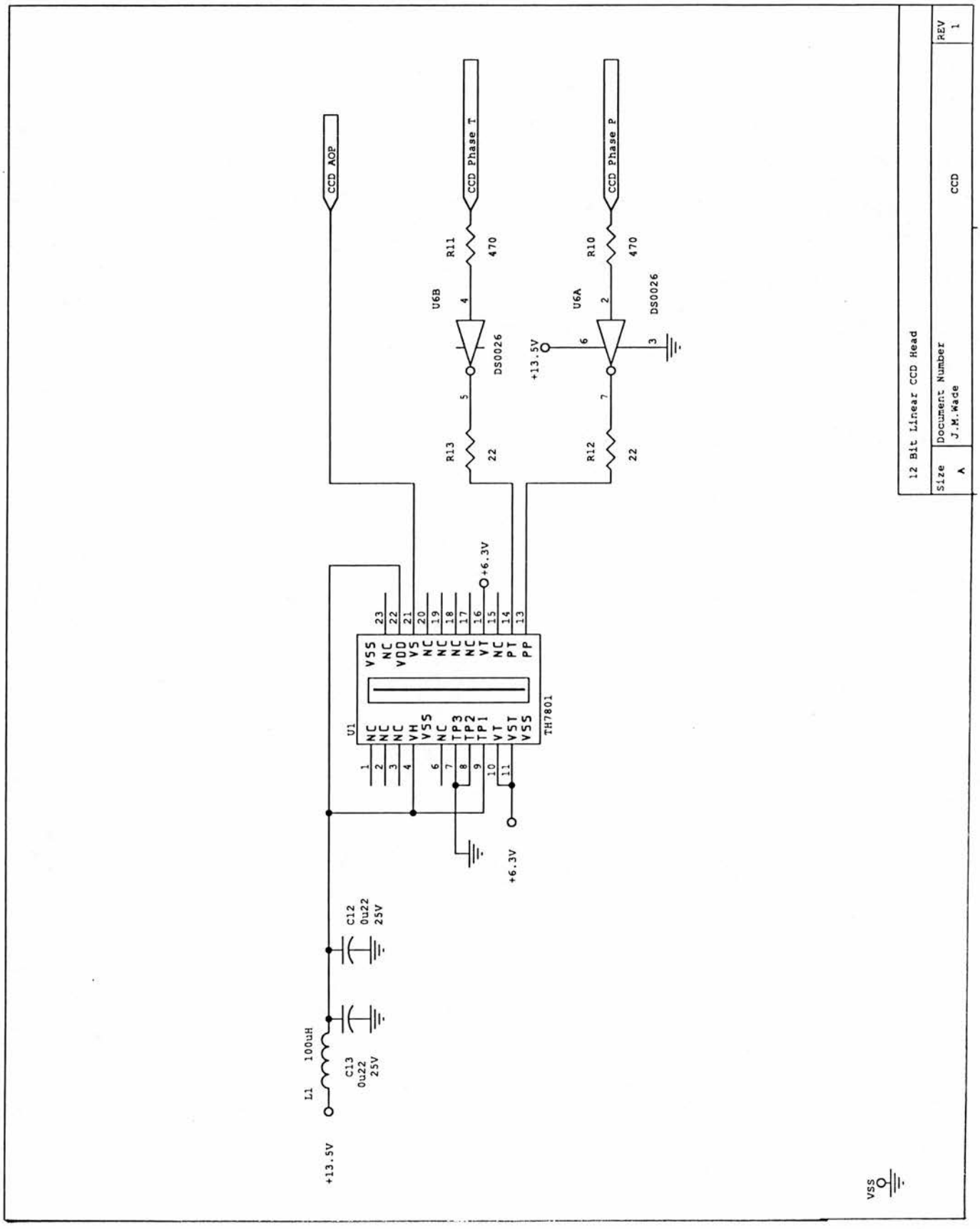


Figure 4.3.5. CCD Circuit Diagram.

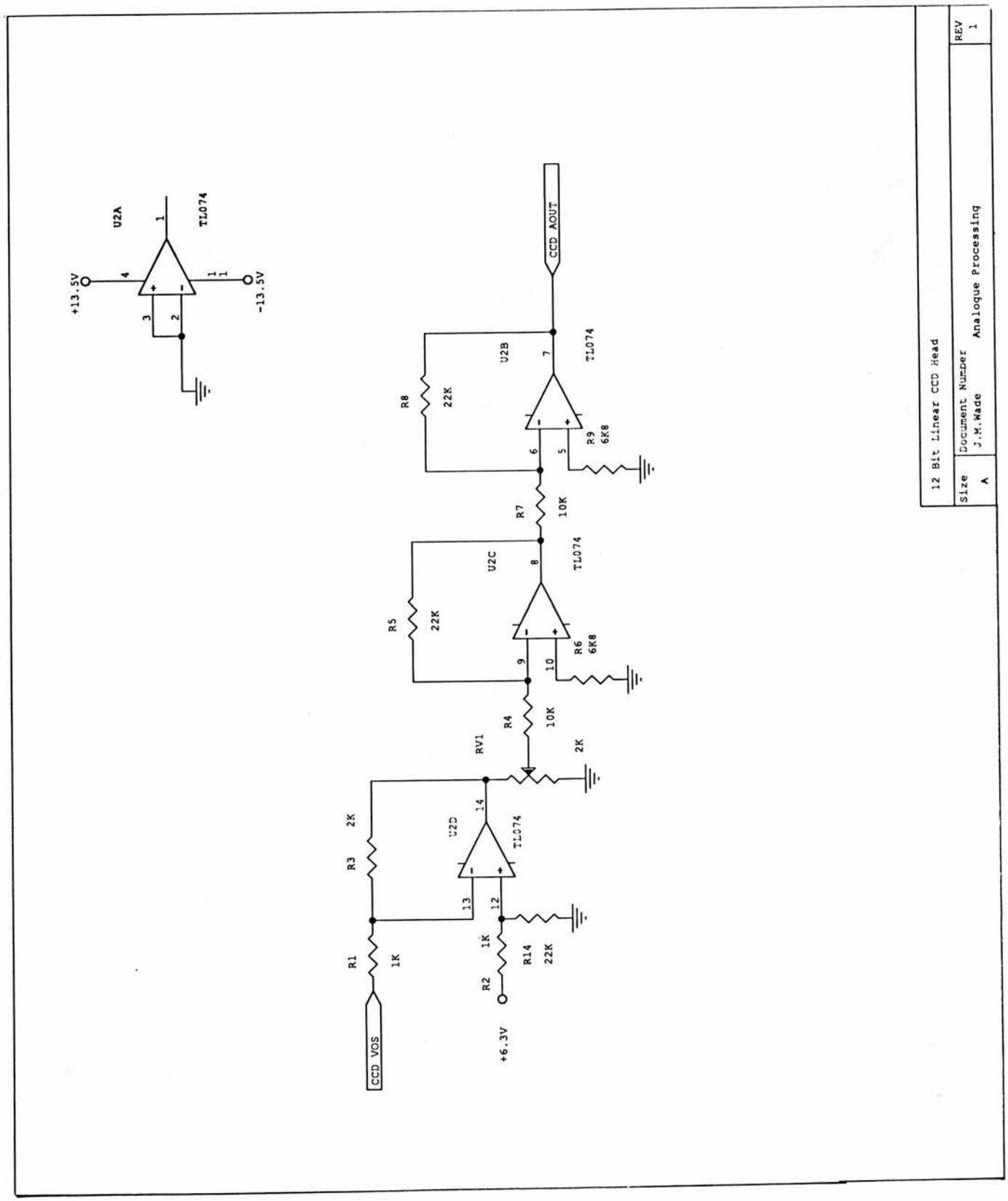


Figure 4.3.6 Analogue Processing Circuit Diagram.

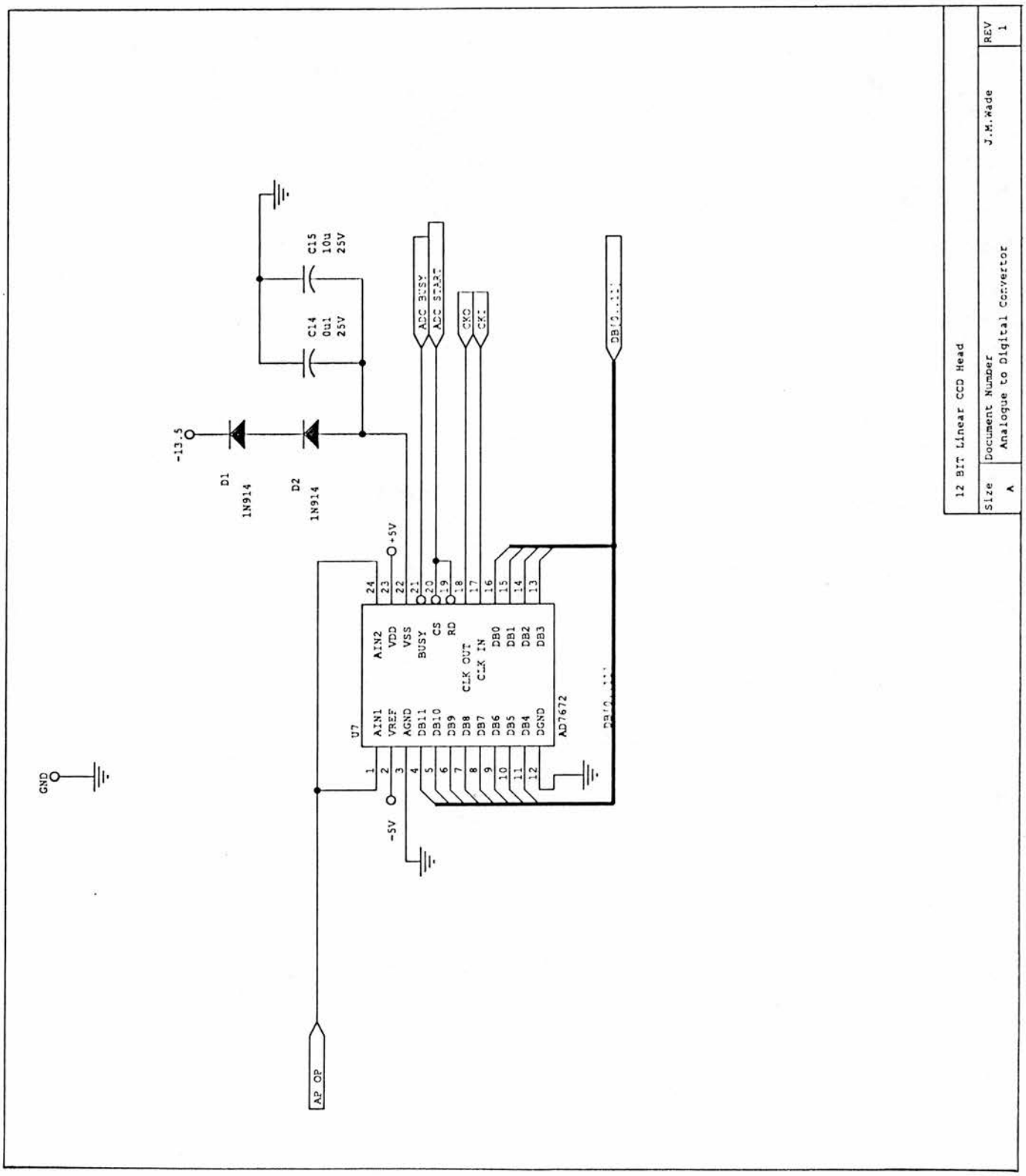


Figure 4.3.7. ADC Circuit Diagram.

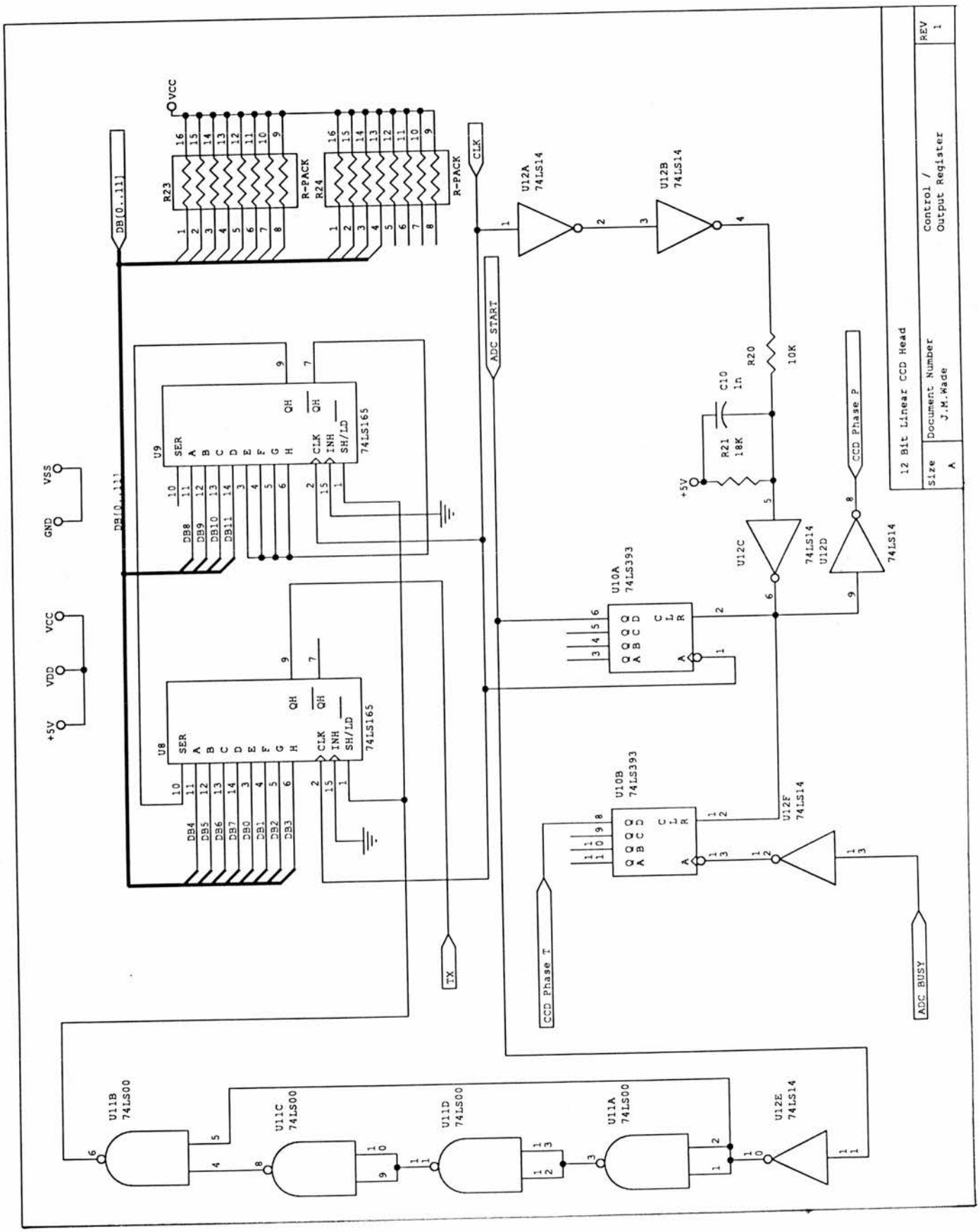


Figure 4.3.8 Control / Output Register Circuit Diagram.

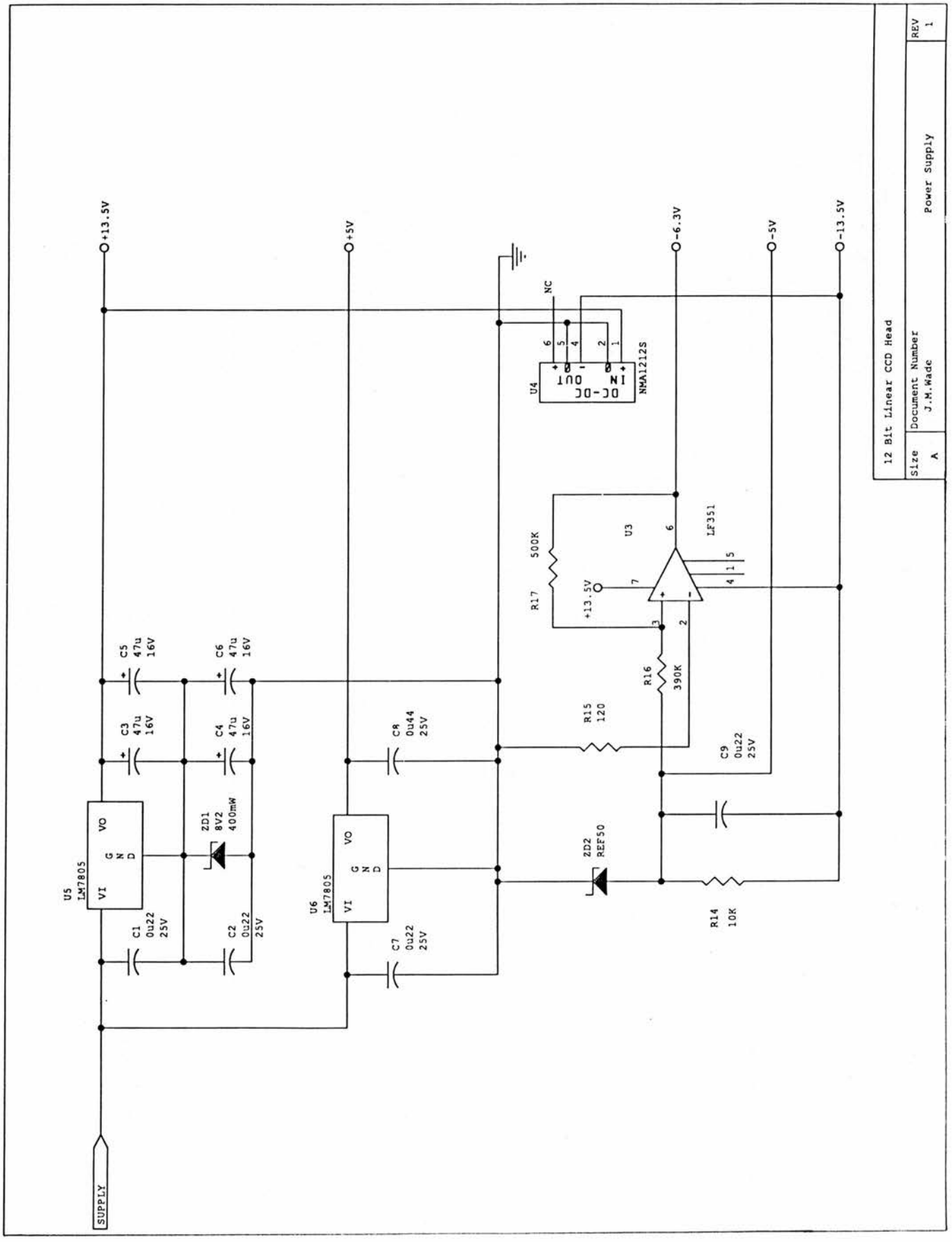


Figure 4.3.9. Power Supply Circuit Diagram.

CCD Camera Component List. Sheet 1 of 2

Item	Quantity	Reference	Part
1	6	C1,C2,C7,C9,C12,C13	0u22
2	4	C3,C4,C5,C6	47u
3	1	C8	0u44
4	1	C10	1n
5	1	C14	0u1
6	1	C15	10u
7	2	D1,D2	1N914
8	1	JP1	HEADER 2
9	1	L1	100uH
10	1	Q1	2N7000
11	2	R1,R2	1K
12	2	RV1,R3	2K
13	4	R4,R7,R14,R20	10K
14	3	R5,R8,R14	22K
15	2	R6,R9	6K8
16	2	R10,R11	470
17	2	R12,R13	22
18	1	R15	120
19	1	R16	390K
20	1	R17	500K
21	1	R21	18K
22	1	R22	220

Figure 4.3.7A COMPONENT LIST.

CCD Camera Component List. Sheet 2 of 2.

Item	Quantity	Reference	Part
23	2	R23,R24	8-SIL 47K
24	1	U1	TH7801
25	2	U2	TL074
26	1	U3	LF351
27	1	U4	NMA1212S
28	2	U5,U6	LM7805
29	1	U6	DS0026
30	1	U7	AD7672
31	2	U8,U9	74HCT165
32	1	U10	74HCT393
33	1	U11	74HCT00
34	1	U12	74HCT14
35	1	U13	HFBR2521
36	1	U14	HFBR1521
37	1	ZD1	8V2
38	1	ZD2	REF50

Figure 4.3.7B. COMPONENT LIST

4.6 BIBLIOGRAPHY

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