Temporary formation of highly conducting domain walls for non-destructive read-out of ferroelectric domain-wall resistance switching memories

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Abstract: Erasable conductive domain walls in insulating ferroelectric thin films can be used for non-destructive electrical readout of the polarization states in ferroelectric

memories. Still, the domain wall currents extracted by these devices have not yet reached the intensity and stability required to drive read-out circuits operating at high speeds. This study demonstrated non-destructive read-out of digital data stored using specific domain wall configurations in epitaxial $BiFeO_3$ thin films formed in mesa-geometry structures. Partially switched domains, which enable the formation of conductive walls during the read operation, spontaneously retract when the read voltage is removed, reducing the accumulation of mobile defects at the domain walls and potentially improving the device stability. Three-terminal memory devices produced 14 nA read currents at an operating voltage of 5 V, and operated up to T = 85°C. The gap length can also be smaller than the film thickness, allowing the realization of ferroelectric memories with gate dimensions below 100nm.

Ferroelectric polarization can be reversed using either out-of-plane or in-plane electrical fields, enabling the application of ferroelectric materials in spatial visualization, electrochemical sensors, and nonvolatile ferroelectric memories with ns-to-ps-scale programming times, almost unlimited cycle endurance, and low energy consumption[1-5]. The domain size of the memory cells can be as small as a few nanometres[6,7], which is favourable for terabit-density integration. However, in ferroelectric memories that are compatible with complementary metal-oxide-semiconductor (CMOS) technology, the information stored in the ferroelectric domains is extracted via a destructive read-out process based on charge integration, which requires a minimum lateral memory cell size of 250 nm[3,4]. Alternative nondestructive readout methods that use mechanical probes to scan the ferroelectric surface can extract information from smaller domains[8-12] but are incompatible with current CMOS technology[13].

Several groups have recently reported electrical conductivity from the domain walls in insulating ferroelectric materials that may be used for electrical readout of the polarization states in ferroelectric memory devices[14-19]. $BiFeO_3$ (BFO) thin films are attractive for these applications because their 71°, 109° and 180° domain walls have demonstrated stable currents of up to 200 pA[19-23], which may be useful for domain-wall-type resistance switching random-access memories. However, this current value is still not sufficient to drive readout circuits during high speed operation: according to the Johnson-Nyquist limit, a minimum current of 0.1 μA is required to obtain read times of 10 ns[24,25]. However, local enhancement – by several

orders of magnitude – of the currents generated in the 71° domain walls of BFO films has recently been observed in a transmission electron microscopy (TEM) study[26].

In-plane reading and writing for domain-wall memories using an epitaxial BFO film has been recently reported[1]. Because an in-plane electrical field was applied between two top electrodes separated by a gap length l, which is much larger than the BFO film thickness d, a triangular 71° domain can be written through the entire thickness of the BFO thin film in a single-domain pattern. The written polarization remained stable for over 2 h and could subsequently be read out via current conduction along the conductive walls located along the domain side boundaries. The detected currents were only 5–20 pA, however, which are too low to operate sense amplifiers at sufficiently high speeds. While this is a step forward in domain-wall type resistance switching memory technology, the technology suffers from a fundamental reliability issue related to instability of the charge-uncompensated persistent domain boundaries, in addition to its ultimately limited scalability because $l >> d$.

Here, we demonstrate an advanced working prototype of an in-plane multi-domain ferroelectric memory device in which rectangular-shaped written domains in tiny mesa-structured cells can be read out nondestructively via temporary and partial switching of the domains within the gap where $l << d$. The conductive walls appear under application of a short-time read field that is larger than the coercive field of the domain, but they disappear immediately after read field termination. The detected current was as high as 14 nA. The temporary presence of these domain walls during only reading avoids mobile defect accumulation on the walls, which significantly

improves device reliability. This intriguing phenomenon represents a step forward towards memory device applications.

Simulation of the creation of charged walls

To provide proof-of-concept, planar-type devices are first fabricated on 35-nm-thick epitaxial $(001)_{pc}$ BFO films (where "pc" denotes pseudocubic) grown on (001) $SrTiO_3$ (STO) substrates. In-plane transverse domain switching occurs when a horizontal electrical field (***E***) is applied along the $[100]_{pc}$ direction between the two top electrodes (TE1 and TE2), which are separated by a gap width/length of *w*/*l*, as shown in Fig. 1a. The film has polar axes along its $<111>_{pc}$ directions with virgin polarizations consisting of the 71°, 109° and 180° domain walls[27,28], as indicated by the light cyan-coloured arrows passing through the entire film thickness. The virgin polarization (which corresponds to written information) can then be read out through transient creation of conductive charged walls via a partial domain reversal near the film surface when ***E*** is applied antiparallel to the in-plane polarization component (***P***), as indicated by the wine-coloured arrows between TE1 and TE2. The purple dashed field lines shown in Fig. 1a indicate the calculated switched regions near the film surface that penetrate into the interior under applied voltages of 1.7–3.4 V. In these calculations, the read voltage was applied to TE1 while TE2 was grounded. The partially switched domains can form charged walls with high readout currents (signifying data "1") through rotation of the local polarization within the film matrix (Fig. 1a, right panel). These unscreened charged walls disappear immediately after removal of the read

voltage because of domain back-switching driven by the strong depolarization field (~14.6 MV/cm if unscreened). When the information is written in the opposite manner, i.e., with $\boldsymbol{P}$ // $\boldsymbol{E}$ (signifying data "0"), charged wall formation does not occur upon application of the read voltage and thus no readout current is produced.

Nanodevice fabrication

Epitaxial $(001)_{pc}$ BFO thin films with thicknesses of 35 and 120 nm were grown on (001) STO substrates by pulsed laser deposition (see Methods). The topographic atomic force microscopy (AFM) image in Fig. 1b (left panel) shows terraces of atomic steps with root-mean-square roughness values of 0.17 nm on the 120-nm-thick film. Reciprocal space mapping of the $(103)_{pc}$ reflection (right panel) confirmed heteroepitaxial growth[29]. Other X-ray diffraction (XRD), AFM and TEM images are shown in Supplementary Fig. S1a, b and Fig. S2a–c. After film deposition, TE1 and TE2 were deposited and were patterned by electron beam lithography and ion milling (see Methods). Figure 2a–d show scanning electron microscope (SEM) images of the fabricated nanodevices. As-grown domain patterns along the $[100]_{pc}$ direction (i.e., the preliminary written information) can be determined using in-plane piezoresponse force microscopy (PFM) phase imaging. Figure 2e–h show the 180° phase shifts of the two domains (indicated by the black colour in Fig. 2e and h versus the white colour in Fig. 2f and g) that are confined within the nanogaps with polarizations pointing from TE1 to TE2 (positive domains; data "0"), and vice versa (negative domains; data "1"), respectively. The PFM phase contrast shows the in-plane

projection of the as-grown 71° domains (Supplementary Fig. S3a–c, Fig. S4a–f and Fig. S5)[30].

"On" currents

Figure 2i–l show the quasi-static current-voltage (*I-V*) curves of the 35-nm-thick BFO devices shown in Fig. 2a–d, respectively, with *l* increasing from 63 to 164 nm at *w* of 52 nm. All *I-V* curves show diode-like asymmetric and hysteretic behaviour, where the diode-like polarity is determined by the polarization direction. For example, the "on" and "off" currents appear when ***E*** is applied antiparallel and parallel to ***P***, respectively, as indicated by the coloured arrows in Fig. 2i–l. These results are in accord with the principle of charged wall formation shown in Fig. 1a.

Figure 3a shows 100 cycles of the hysteretic *I-V* curves for the positive domains that were shown in Fig. 2e. There is a high probability within each loop that domain switching will occur at the coercive voltage V_c (the voltage at which a current jump occurs), and V_c follows a Lorentzian distribution, as shown in the inset, demonstrating the random nature of the domain nucleation at the TE edges[2,31,32]. $|V_c|$ increases with increasing *l*, as indicated by the blue circles in Fig. 3b. Figure 3c shows the on-state current variation at 4 V as a function of *l* (*w* = ~50 nm). The wall currents have been variously reported to be ohmic[33], Schottky-like[15,20,21] or space-charge-limited (SCL)[20]. The "on" currents here can be fitted using the $I \propto V^n$ power law, as indicated by the black dashed lines in Fig. 2i–l, where n = 2.2 – 2.6. This is a well-known

characteristic of the SCL mechanism[20]. The "on" current increases greatly with decreasing l, following an $I \propto l^{-3}$ relationship, as shown in Fig. 3c (solid line).

Figure 3d shows the hysteretic current loop of the device shown in Fig. 3a that was achieved by application of periodic read-write operations using the pulse sequence shown in the inset. In this test, the write voltage (V_w) was programmed to change from 3 V$\rightarrow$−3 V$\rightarrow$3 V in steps of 0.1 V under fixed read voltages (V_r) of −1.5 V. In this case, the domain pattern was manipulated using write pulses before the common reading operation was performed. The loop clearly indicates that the conduction path was created at −2.5 V (dramatic current increase) but disappears at −1 V (dramatic current drop) because of domain back-switching. The disappearance time varies from 16 ns to 1 h (Supplementary Fig. S6a, b and Fig. S7a, b), depending on the write field strength and time. Rapid restoration of the polarization (disappearance of the domain wall) after read voltage termination can prevent the accumulation of oppositely charged defects, which may screen the polarization charges[34]. Figure 3e shows the switching time dependence of the readout "on" current at 2.8 V ($<|V_c|$) when the switching voltage was higher than V_c (= 3.2 V) (see Methods). The current jumps from "off" to the "on" state at a characteristic domain switching time t_0, which can be described using the Kolmogorov-Avrami-Ishibashi (KAI) model with the equation $I = I_{on}\{1-\exp[-(t/t_0)^2]\}$[35], where I_{on} is the "on" current at 2.8 V, as shown by solid-line fitting of the data. Using these plots and Merz's law[36], an activation field of 37.5 MV/m was derived (Supplementary Fig. S8a). Figure 3f shows the endurance test results up to 10^7 cycles of "on" and "off" currents using ±4 V write and read pulses (with

amplitudes >|V_c|) with a 1 kHz repetition rate in full duty (see Methods). A stable on/off current ratio of 100 was confirmed.

As the film thickness increased up to 120 nm, similar *I*-*V* curves and an *I*-*l* dependence at 5 V for $w = 44$ nm were also observed, as shown in Fig. 4a, where the "on" current density increases by approximately five times (see Methods and Supplementary Fig. S8b). From fitting of the data according to $I \propto l^{-3}$ (the red line in Fig. 4a, right panel), a 1 μA readout current can be expected at $l = 21$ nm when $V_r = 5$ V, or at $l = 7.2$ nm when $V_r = 1$ V. This behaviour is highly promising for terabit-density integration and low power consumption, because higher density (smaller *l*) leads to higher readout currents and reduced read voltages.

PFM and conductive AFM (CAFM) tests were performed on a larger device with $w/l = 1.5$ μm/0.6 μm to confirm the high domain wall conductivity directly. After device poling at −18 V for 10 s, the high-field charge injection can temporary stabilize the partially-switched 71° domains for over 1 h (Supplementary Fig. S7a, b), which allowed the capture of the PFM and CAFM images. Figure 4b shows an in-plane PFM phase image of two head-to-head 71° triangular domains located between TE1 and TE2. The concurrently captured CAFM image (Fig. 4c) of the same region at a tip field of −140 kV/cm (see Methods) clearly shows the much higher electrical conductivity of the entire domain-wall region. The domain tip region (crossed by the green dotted line, *n*) shows a higher current (~120 pA) than the bottom region (crossed by the dark yellow dotted line *m*; ~63 pA).

Write and read in three-terminal devices

To write arbitrary data into the memory cell and demonstrate the broad operating voltages, two three-terminal memory device schemes are proposed, which are intended to operate when $|V_r| > |V_c|$ (Scheme I) and $|V_r| < |V_c|$ (Scheme II) (left panels, Fig. 5a, b, respectively). In both cases, memory cells were fabricated with mesa structures by etching 120-nm-thick BFO films to depths of 105 nm. Pt layers were deposited and etched to produce left (**L**), middle (**M**) and right (**R**) electrodes, as shown by the planar SEM image in Fig. 5c (left panel). $V_{\mathbf{LR}}$, for example, denotes the voltage that is applied to **L** with **R** being grounded and **M** floating. **L** and **R** form a parallel-plate capacitor-like structure that can screen the domain boundary charge efficiently and domain back-switching after the write operation is thus prohibited. For Scheme I, a write voltage of $V_{\mathbf{LR}} = -8$ V is applied to switch the whole domains between **L** and **R,** for which the polarization is represented by yellow arrows in Fig. 5a (write "1"). In this device geometry, both **L** and **R** are partially extended over the cell surface, which concentrates the read field between the two ends of the top electrodes. V_r is applied either between **L** and **M** or between **M** and **R**. When $V_{\mathbf{LR}}$ and V_r have opposite signs, the charged domain walls appear because of partial domain switching within the gap. These walls disappear on termination of V_r because of domain back-switching. The left-hand panel of Fig. 5a shows the nondestructive readout of a data "1" when $V_r > V_c$ (read "1"). The middle panel shows *I*-*V* curves for a device with gap distances of l_{LM} = 82 nm and l_{MR} =120 nm under V_r of 5 V and 7 V, respectively, where the repeatable current jump that occurs at V_c = 5.2 V for the l_{MR} device predicts abrupt formation of

the conductive wall. The maximum "on" current is ~14 nA (red *I*-*V* curves). When the write $V_{\mathbf{LR}}$ was changed to +8 V (write "0"), no switched domains formed, and thus no high wall currents were observed during the read operation. The observed "off" current of ~5 nA (blue *I*-*V* curves), however, is ascribed to the device leakage current induced by process damage (read "0"). Both the "on" and "off" currents are stable over time, as shown in the right panel, and are proportional to the electrode width (Supplementary Fig. S9) with a ratio of ~3. The wall currents in an insulating two-terminal nanodevice did not show any notable changes upon variation of the environmental pressure from 1 to 1.4×10^{-7} bar (Supplementary Fig. S10a), but showed thermally activated behaviour with activation energy of 0.16 eV (Supplementary Fig. S10b). This behaviour corresponds to the hopping conduction of the SCL mechanism (Supplementary Fig. S11)[36].

For scheme II (where $|V_r| < |V_c|$), a device structure without **L** and **R** extensions could be used, as shown in Fig. 5b. In this case, a presetting voltage of V_p = + 8 V across l_{LR} (left panel) is applied once to polarize the BFO uniformly in the same direction. Subsequently, the regions between **L** and **M** or **M** and **R** can be written independently with a $|V_w| > |V_c|$, which can then be read out at $|V_r| < |V_c|$. In this case, the conductive walls created by the application of V_w are retained even after removal of the V_w because of improved compensation of the domain boundary charges at the **L**/BFO and BFO/**R** interfaces. Subsequent application of V_r ($|V_r| < |V_c|$) does not create additional conductive walls but simply reads out the wall current. The middle panel shows the *I*-*V* curves for both sides of the device when l_{LM} = 129 nm and l_{MR} =

100 nm, where the "off" currents suddenly increased at −2.2 V, thus predicting the charged wall formation. The stability of these walls was further confirmed by retention of the "on" currents when the voltage is swept back to a positive-bias region, where the "on" current decreased abruptly at 1.6 V for the **L**-**M** device but at 0.69 V for the **M**-**R** device (the inset shows the magnified curves), thus predicting the disappearance of the conductive walls. The bistability of the wall currents in this scheme differs from that in Scheme I. The on/off currents at −1.5 V are stable over time at either room temperature (right panel, Fig. 5b) or 85°C (Supplementary Fig. S12a, b). The in-plane PFM phase images in Fig. 5c and Supplementary Fig. S13a–c confirm switching of the stable 71° domain with a rectangular shape between **L** and **R** (the middle panel **M** was removed for this PFM test). Additional endurance testing of the mesa structure showed no polarization fatigue for cycle numbers of up to 10^9 (Supplementary Fig. S14a, b).

Discussion

According to the Landau-Lifshitz-Kittel law[37], the dependence of the switched domain thickness (h) on length (l) is found to be $h = 1.5\ \mathrm{nm}^{1/2}\ l^{1/2}$. Because the coercive field of the BFO was assumed to be 20–25 MV/cm, we simulated the nonlinear V_c-l dependences shown by the solid lines in Fig. 3b (red line) and 4a (right panel, blue line). The switching field under the read voltage shows maximum values at two regions near the TE1 and TE2 edges that decay rapidly towards the middle gap with increasing l (Supplementary Fig. S15a–d).

Finally, while the memory devices with planar geometries shown in Fig. 2a–d have the merit of easy fabrication[1], they have several problems including difficulties in writing bipolar information into multi-domain films with sufficiently long retention times[38] and obtaining sufficiently high readout currents ($I \propto V_r^2/l^3$). The persistent presence of uncompensated charged walls also leads to problems of mobile defect agglomeration[33,39,40]. In contrast, the mesa-type device shown in Fig. 5a is completely free from these concerns, which even permits a passive cross-bar architecture without involving the voltage-time dilemma (see Methods)[41,42].

In summary, in-plane readout currents that are ascribed to penetrating domain walls along ferroelectric BFO film surfaces are demonstrated for ferroelectric resistance switching nanodevices with excellent scalability and reliability[43]. Conductive walls are only formed when the read voltage is applied, for which the polarity is opposite to that of the write voltage, but the walls disappear on termination of the read voltage. This operating principle alleviates potential problems related to the instability of uncompensated charged domain walls that persist even after read voltage termination[1]. In contrast, the written domain information can be retained stably by efficient charge compensation at the side electrode interfaces in the mesa device structure. Other potential applications of these domain-wall engineered ferroelectric nanodevices include the detection of light illumination, anisotropic magnetoresistance, and photovoltaic currents[27,44,45].

Methods

Film growth. Epitaxial BFO films were deposited on (001) STO substrates by pulsed laser deposition using a KrF excimer laser operating at a wavelength of 248 nm. The laser (6 Hz) was focused with a power density of 2.8 J/cm^2 on a ceramic $Bi_{1.1}FeO_3$ target at an oxygen pressure of 3 Pa. The typical film growth rate was ~1 nm/min. Films with thicknesses of 35 nm and 120 nm were grown at 602°C. XRD patterns were collected by θ-2θ scanning and reciprocal space mapping methods using a Bruker D8 Advance X-ray diffractometer with Cu-K_α radiation at 40 kV and 40 mA.

Nanodevice fabrication. After BFO film growth, 30-nm-thick Pt top electrode layers were grown at 400°C on the BFO films by magnetron sputtering (PVD-75, Kurt J. Lesker). Subsequently, 200-nm-thick poly(methyl methacrylate) photoresist layers were spin coated onto the film surfaces. The TE1 and TE2 electrode patterns were formed by electron beam lithography (EBL; 6300FS, JEOL) with overlay accuracy of 20 nm. After patterning, 25-nm-thick Cr mask layers were deposited by thermal evaporation (NANO 36, Kurt J. Lesker) and a lift-off technique. Finally, the $Pt/BiFeO_3$ region that was not protected by the Cr mask layer was removed by ion milling using a reactive ion etching system (RIE-10NR, Samco). The as-formed nanodevices were checked using SEM (Sigma HD, Zeiss) images. The BFO film was slightly over-etched during removal of the Pt diffusion layer (~2 nm) to ensure complete Pt removal for lowering of the leakage current, which left 2–3 nm-sized

holes (shown as dark spots in Fig. 2a–d) on the film surface (Supplementary Fig. S1b). This over-etching induced leakage problems in the device in the "off" state.

TEM images. The sample was prepared by a focused ion beam method (using ~100 nm lamellae). High-resolution TEM (HRTEM) imaging and selected-area electron diffraction (SAED) processes were performed using a Philips CM200 field emission gun operating at 200 kV. The HRTEM image was Fourier-filtered to minimize the contrast noise.

PFM and CAFM characterization. The film morphology was measured using an AFM in Scanasyst-air mode (Bruker Icon) under ambient conditions using a silicon tip with radius of 2 nm. PFM imaging of all domains was performed using a contact PtIr-coated silicon tip with radius of 20 nm, a force constant of 2.8 N/m, and an alternating current (AC) frequency of 75 kHz and an amplitude of 10 V. The exposed wall currents at the film surface were investigated using CAFM in contact mode under a nominal electric field of −140 kV/cm applied between TE1 and the AFM tip with both the tip and TE2 being grounded.

Electrical characterization. All nanodevices were characterized electrically under N_2 environmental pressures that ranged from 1 to 1.4×10^{-7} bar. Each *I-V* curve was measured using an Agilent B1500A semiconductor analyzer operating in voltage sweep mode with a sweep time of 90 s. For fatigue (endurance) testing, square pulses

with rise times of 2 ns at frequencies of either 1 kHz or 1 MHz were supplied by a two-channel Agilent 81110A pulse generator. After each fatigue period of 1 s, the sample was relaxed intermittently at 0 V for 3 s. This time relaxation can effectively mitigate the long-term space-charge accumulation that causes the coercive voltages of the charged domain walls to shift. The steady-state "on" current transient with time was observed directly using a LeCroy HDO6054 oscilloscope. For the domain switching performance, a long-time read pulse ($|V_r| < |V_c|$) is superimposed over a short-time write pulse to hold the switched domain on for the "on" current measurement. During the domain switching time, the internal series resistance of the oscilloscope was 50 Ω, but it was increased to 1 MΩ when measuring the readout current to reduce the noise level to ~0.1 nA.

Finite element simulation. The stray electric field distribution within the nanogaps under applied E was analysed via a finite element simulation using the electrostatics interface tool of COMSOL, which solved the combined equations of $\nabla \cdot D = \rho$, $D = \varepsilon_0 \varepsilon_r E$, and $E = -\nabla V$ according to the three-dimensional Gauss law, where D is the electric displacement, ρ is the space-charge density, and V is the electric potential. The dielectric permittivities of BFO and STO were assumed to be 93 and 332, respectively. A finite element simulation (Fig. 1a, purple dashed lines) and high-field I-V curves (Supplementary Fig. S8b) consistently predicted expansion of the switched domain into the film interior with increasing applied voltage until the bottom portion of the domain wall touches the substrate. Under these circumstances, the current along the

bottom wall is prohibited and only the domain side boundaries can thus provide the current path, which seriously limits the total achievable current for the thin film (35 nm) shown in Fig. 3c. This limitation is avoided in the thicker film (120 nm) shown in Fig. 4a.

Cross-bar architecture. After the memory read process is terminated, the sneak path that arises from the conductively charged wall in each cell would be cut off in a nondestructive readout technique. This operating scheme reduces the risk of involving the circuit sneak current in a similar manner to the complementary resistive switches consisting of two anti-serial memristive elements that are used when the devices are integrated using a cross-bar array configuration[41]. In the proposed cross-bar architecture, parallel wire-shaped electrode rows contact the **L**s of all the densely arrayed cells, and the other **M**s and **R**s can be interconnected using hole-type contacts with top and bottom perpendicular electrode columns in the case of the three-terminal device shown in Fig. 5a. Fast writing of the domain information does not involve trapping and detrapping of electronic charge in insulators as the resistance mechanism changes. This feature can help to avoid the voltage-time dilemma that occurs in metal/insulator/metal thin-film stacks, i.e., the long retention times of the devices mean that sufficiently high barriers are required to suppress the escape of the trapped electronic charge, which prevents the use of the high currents needed for short read and write pulses at low operating voltages[42].

Data availability. All data generated or analysed during this study are included in this published article (and its supplementary information files).

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Author contributions

A.Q.J. conceived the idea for the work and performed the electrical characterization and part of the PFM characterization, and, in conjunction with D.W.Z., C.S.H, and J.F.S, directed the study and analyzed the results. J.J. performed the BFO nanodevice fabrication process. Z.L.B. grew the films, measured the XRD patterns, and

performed the CAFM measurements. Z.H.C. performed the finite element simulations. L.H. performed part of the PFM measurements, while J.A.S. fabricated the TEM samples, and Q.H.Z. performed the TEM observations. J.J. and Z.L.B. contributed equally to this work. All authors discussed the results. A.Q.J. and C.S.H. wrote the manuscript.

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Figure Captions:

Figure 1 | Creation of charged walls. **a**, Simulated horizontal fields at the middle of the gap with w/l = 50 nm/50 nm at 2.5 V for a 35-nm-thick $(001)_{pc}$ BFO film on a (001) STO substrate (left panel). Purple dashed lines indicate the regions where the applied field exceeds the coercive field of 20 MV/m under various applied voltages. Wine-coloured arrows indicate the partial inversion of the domains under applied $\boldsymbol{E}$ in the film matrix (light cyan-coloured arrows) written by various stimuli. The right panel shows possible rotations between the various domain configurations of r1-, r1+, r2-, r3-, and r4+. **b**, AFM topography (left panel) and reciprocal space mapping from the $[103]_{pc}$ reflection (right panel) from a 120-nm-thick BFO thin film grown epitaxially on a [001] STO substrate.

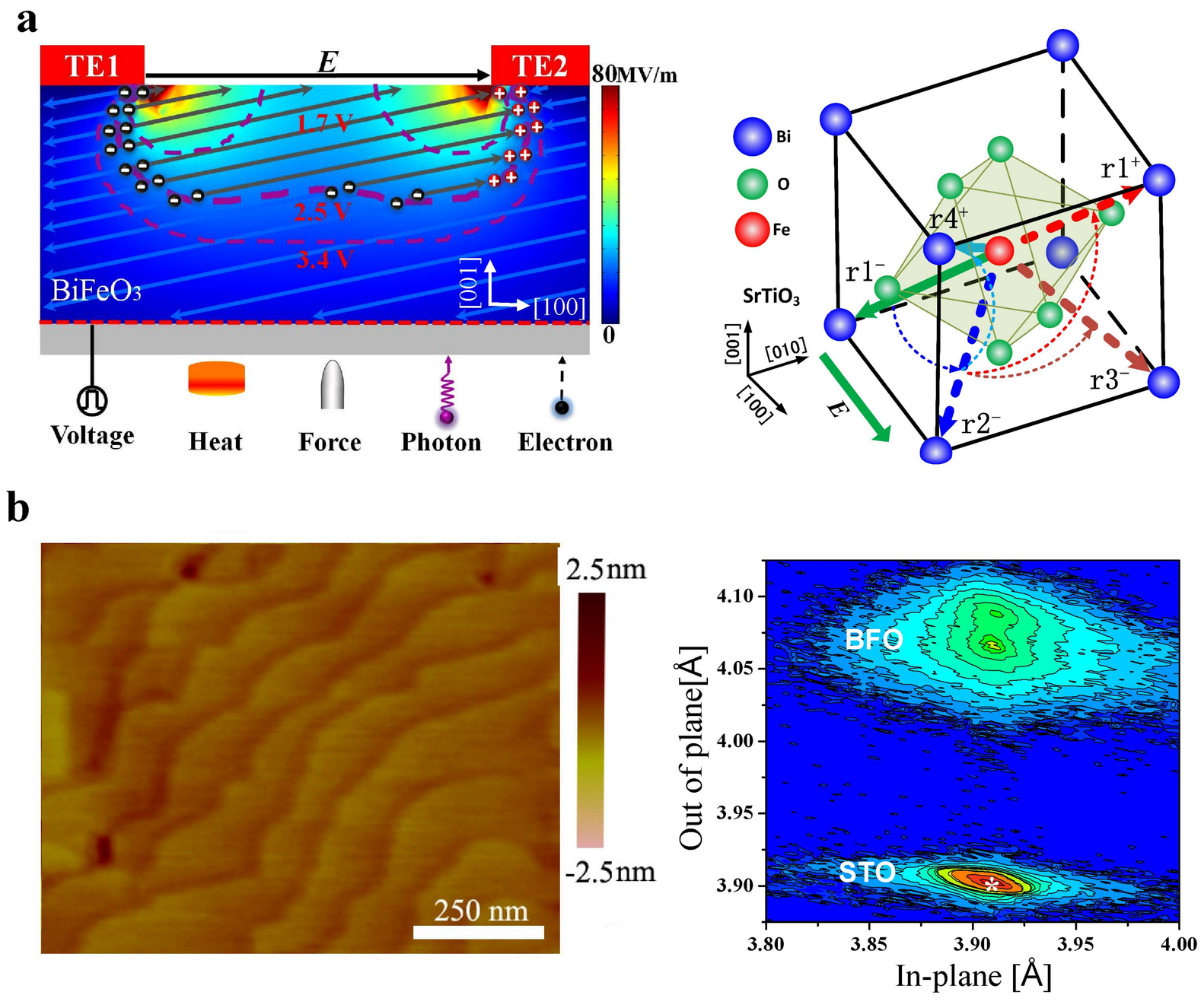
Figure 2 | "On" currents of 35-nm-thick nanodevices. **a**–**d**, SEM images of nanogaps with gap lengths of 63 nm, 97 nm, 136 nm, and 174 nm and widths of ~52 nm. **e**–**h**, In-plane PFM phase images of the positive (dark colour in **e** and **h**) and negative (white colour in **f** and **g**) domains along the applied $\boldsymbol{E}$ direction that are confined within the nanogaps. **i**–**l**, I-V curves for the positive/negative domains above under forward and backward voltage sweeps in the directions indicated by the black arrows, where the on/off currents occur when $\boldsymbol{E}$ is applied antiparallel/parallel to $\boldsymbol{P}$, respectively. The dashed lines indicate the best fitting of the on currents according to the $|I| \propto |V|^n$ power law.

Figure 3 | Domain switching in the 35-nm-thick nanodevices. a, 100 cycles of the

I-V curves shown in Fig. 2i. The inset shows the Lorentzian distribution of V_c. **b**, **c**, Gap length dependences of the coercive voltage and the on-state current at 4 V with *w* = ~50 nm, where the solid lines are fitting results. **d**, Hysteretic *I-V* curve with the sweeping direction indicated by the black arrows for the nanogap shown in **a** during the periodic read-write operations; the voltage sequence is shown in the inset and the read voltage was fixed at −1.5 V. **e**, Switching time dependence of the readout current at 2.8 V for various applied switching voltages for a nanodevice with *w*/*l* = 52 nm/63 nm and V_c = 3.2 V, where the solid lines indicate the best fitting of the data based on the KAI model. **f**, Endurance test results for the on/off currents at ±4 V and 1 kHz for a nanodevice with *w*/*l* = 51 nm/125 nm.

Figure 4 | Wall currents for 120-nm-thick nanodevices and direct proof of these wall currents using scanning probe techniques. a, *I-V* curves for different gap lengths at *w* = 44 nm (left panel). The right panel shows the *l*-dependences of the coercive voltage and the on-state current under a 5 V field, where the solid lines indicate the fitting results. **b**, In-plane PFM phase image of the remaining parts of two retracted 71° domains (left panel) after poling at −18 V for 10 s. The consequent CAFM current map when −140 kV/cm was applied between TE1 and the tip (right panels), where both the tip and TE2 were grounded, confirms the presence of conductive walls across the gap area. The wall currents decay from their heads to their tails as envisioned using the current profiles along the two dotted lines *m* and *n*.

Figure 5 | Read and write schemes for three-terminal BFO memories. a, **b,** The left panels show schematics of memory cells for the operating schemes with readout voltages of $|V_r| > |V_c|$ and $|V_r| < |V_c|$, respectively, where the dotted lines indicate the charged domain walls that are created under the read voltages. Yellow and white arrows indicate the polarization vectors formed by the write and read voltages. The middle panels show the characteristics of double *I*-*V* sweeps in the directions shown by the arrows after application of different write voltages with various nanogap lengths, while the inset in **b** shows a magnified view of the *I*-*V* curves within the framed rectangle. The right panels show the retention data for the "on"/"off" currents after application of write voltages of either ±8 V or ±2.5 V. The read voltages were 7 V (**a**) and −1.5 V (**b**). **c,** Planar SEM image (left panel) of a mesa-structure memory cell in read Scheme II ($|V_r| < |V_c|$) in **b**. The middle and right panels show in-plane PFM phase images of domain variants indicated by arrows after poling at ±8 V between **L** and **R** (after **M** removal).



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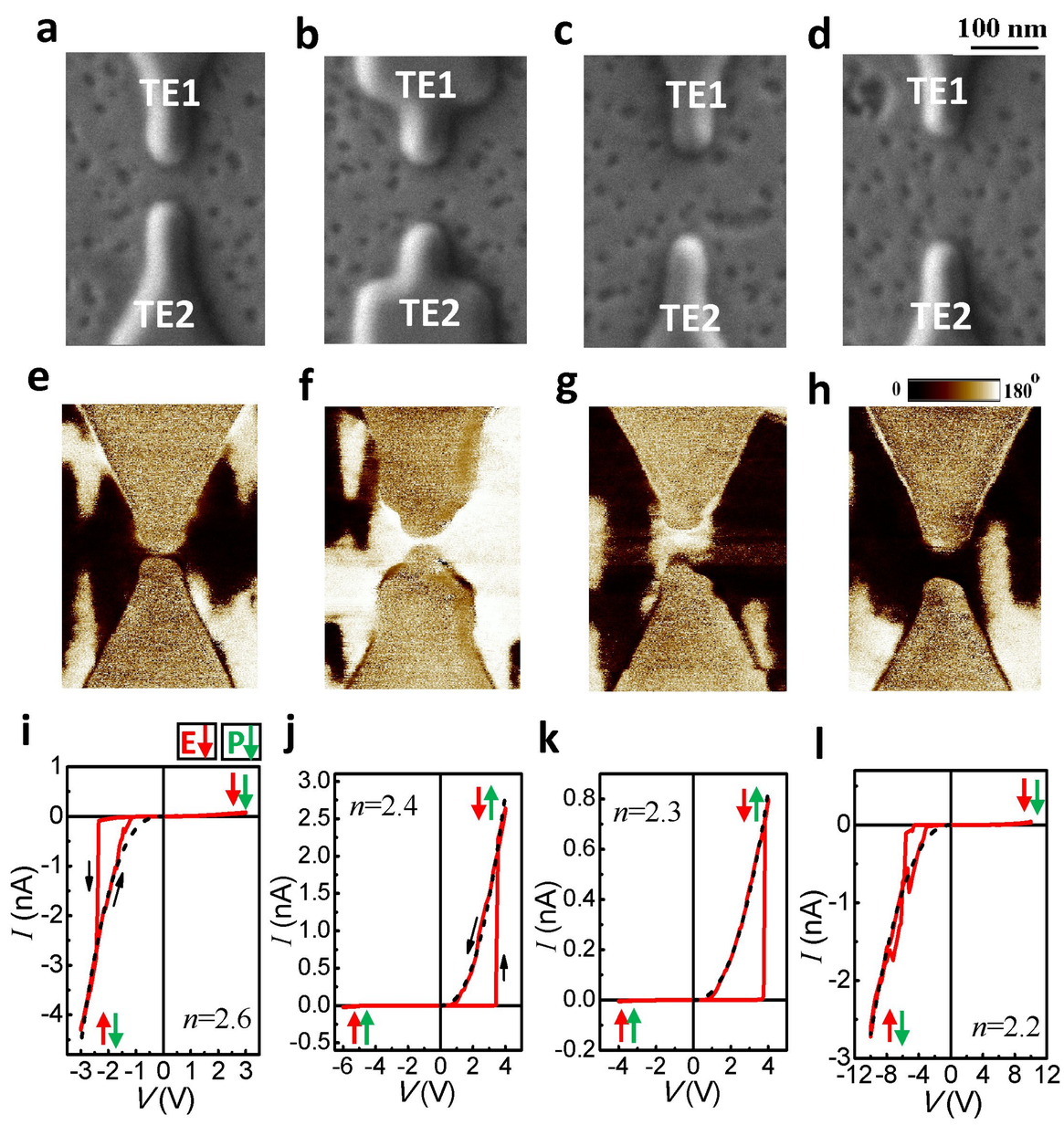

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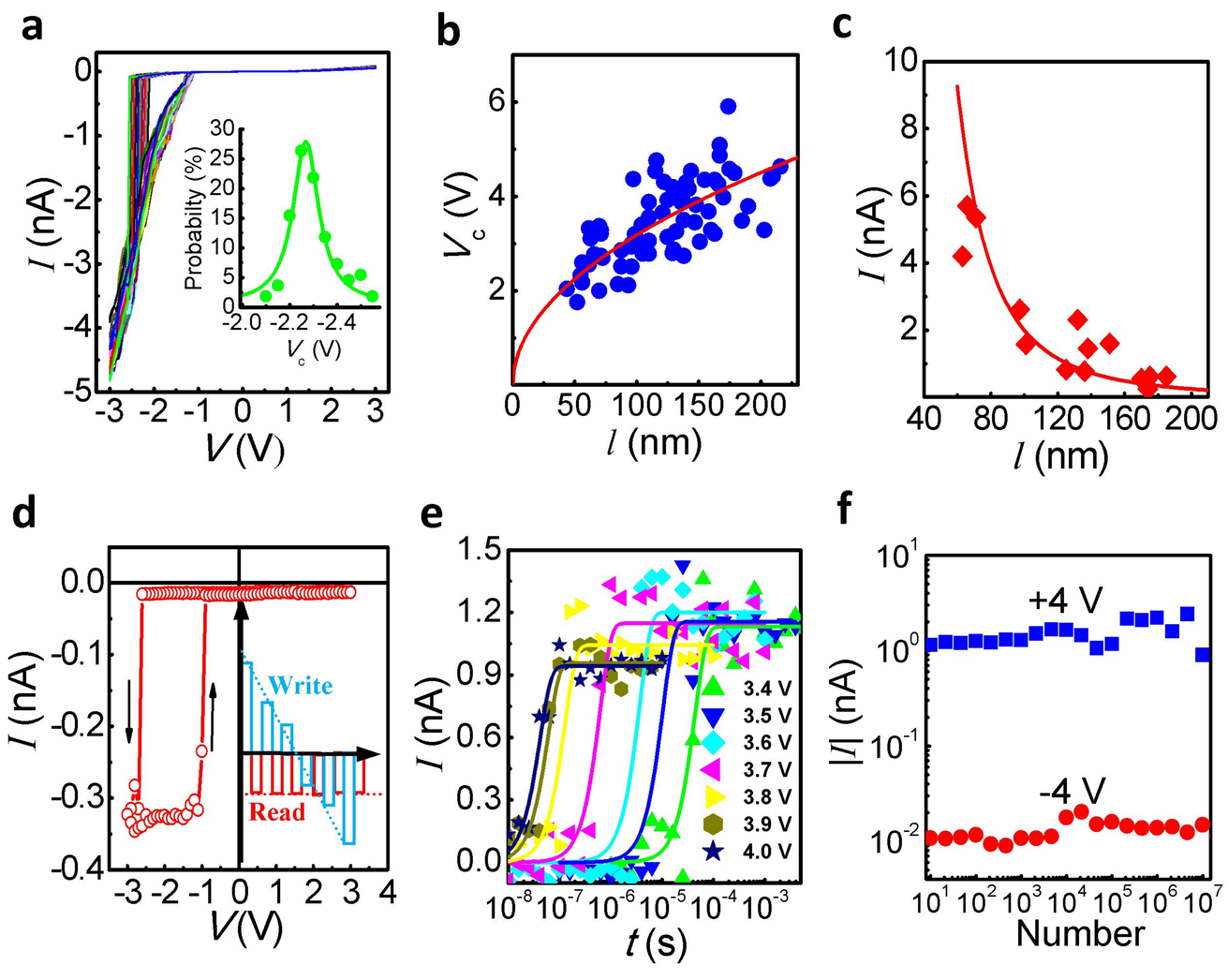

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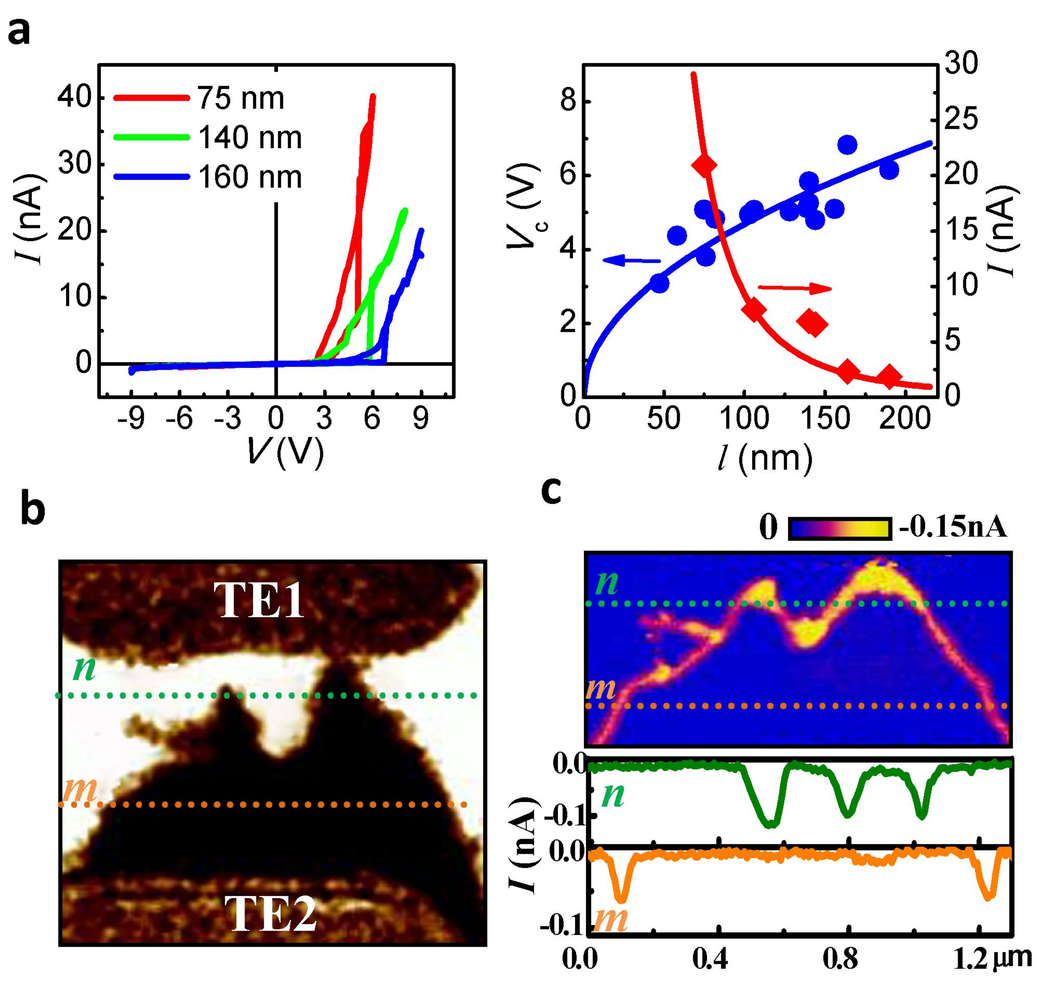

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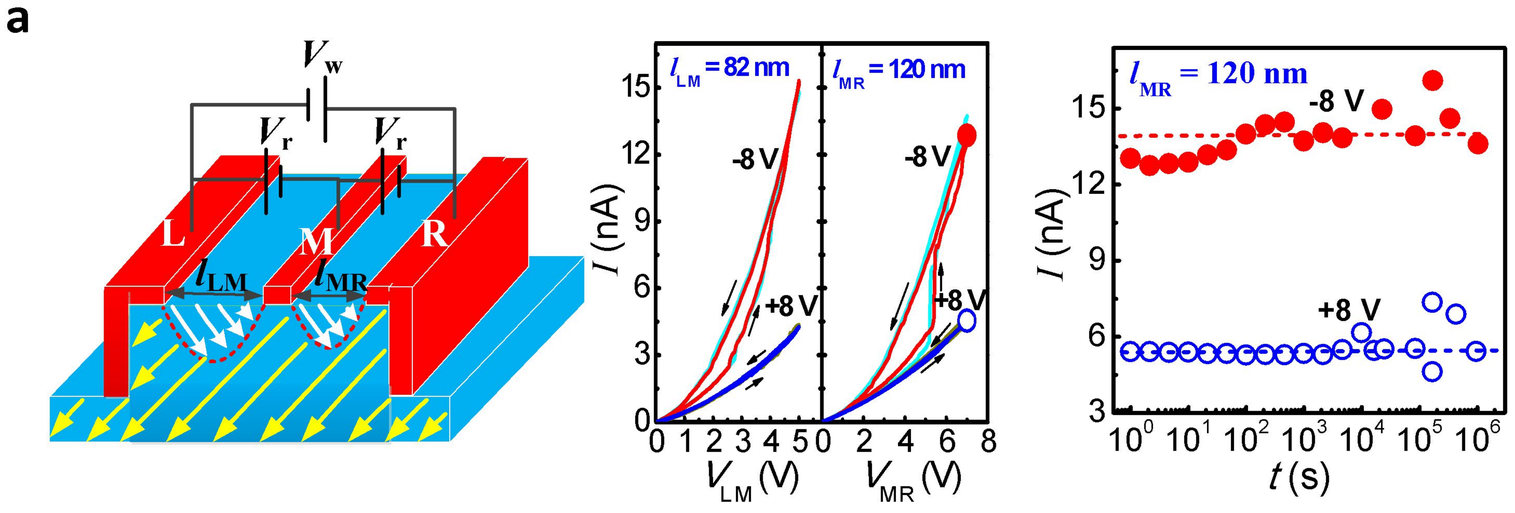

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