Nanoscale Tipping Bucket Effect In A Quantum Dot Transistor-Based Counter

F. Hartmann,[*,†] P. Maier,[†] M. Rebello Sousa Dias,[‡,¶] S. Göpfert,[†] L. K. Castelano,[‡] M. Emmerling,[†] C. Schneider,[†] S. Höfling,[†,§] M. Kamp,[†] Y. V. Pershin,[‖] G. E. Marques,[‡] V. Lopez-Richard,[‡] and L. Worschech[†]

†*Technische Physik and Wilhelm Conrad Röntgen Research Center for Complex Material Systems, Physikalisches Institut, Universität Würzburg, Am Hubland, D-97074 Würzburg, Germany*

‡*Departamento de Física, Universidade Federal de São Carlos, 13565-905, São Carlos, São Paulo, Brazil*

¶*Institute for Research in Electronics and Applied Physics, University of Maryland, College Park, Maryland 20742, USA*

§*SUPA, School of Physics and Astronomy, University of St Andrews, St Andrews, KY16 9SS, United Kingdom*

‖*Department of Physics and Astronomy, University of South Carolina, Columbia, SC 29208, USA*

E-mail: fhartmann@physik.uni-wuerzburg.de

Abstract

Electronic circuits composed of one or more elements with inherent memory – memristors, memcapacitors and meminductors – offer lower circuit complexity and enhanced functionality for certain computational tasks. Networks of these elements are proposed for novel computational paradigms that rely on information processing and storage on the same physical platform. We show a nanoscaled memdevice able to act as an electronic analogue of tipping buckets that allows reducing the dimensionality and complexity of a sensing problem by transforming it into a counting problem. The device offers a well adjustable, tunable and reliable periodic reset that is controlled by the amounts of transferred quantum dot charges per gate voltage sweep. When subjected to periodic voltage sweeps the quantum dot (bucket) may require up to several sweeps before a rapid full discharge occurs thus displaying period doubling, period tripling and so on between self-governing reset operations.

Keywords: quantum dot transistor; memcapacitor; counter; floating gate; quantum capacitance; periodic reset

Although tipping buckets are most commonly known as water park attractions, they are also utilized in sensor applications, for example, in rain gauges.[1] Their ability to reduce the dimensionality and complexity of a sensing problem and transform it into a counting problem makes electronic analogues of tipping buckets useful in complex logic architectures and neuromorphic circuits.[2,3] Necessarily, this transformation requires an autonomous reset which remains a major challenge in the development of nanoscopic counters without the need of external blocks.[4,5] Here, we demonstrate that these goals can be achieved by employing peculiar functionalities of a memcapacitive structure. Memcapacitors are capacitors with memory that together with memristors[6,7] and meminductors form the class of memory circuit elements.[8] The distinguishing feature of these devices is the existence of a physical internal state,[8,9] that remembers the history of signals applied and controls the resistance (for memristors), the capacitance (for memcapacitors) or the inductivity (for meminductors). Bias-dependent resistive switching manifested in hysteretic current-voltage-

curves is characteristic of memristive devices.[7,10,11] Memristive devices are now state-of-the art and have been implemented in various material systems[12] with applications ranging from neural networks[13–17] and unconventional computing[18] to non-volatile memories.[19,20] Compared to memristors, memcapacitors are less studied types of memory circuit elements being introduced and demonstrated more recently.[8,12,21–23] The memory circuit elements are fundamental in the sense that no finite combination of resistors, capacitors and inductors can reproduce their functionality.[12,18] The coexistence of memristive and memcapacitive switching was observed in recent years leading to the definition of memimpedance devices.[24–28] In addition, memcomputers combining memory units with logic processing will be able to adapt to incoming information and retain information on demand on the same physical platform,[18] offering reduced circuit complexity and energy dissipation.

We report a three-terminal memory device – a memcapacitive quantum dot-based counter (QDC) – with unprecedented functionalities grounded on the interplay of two resetting regimes: slow and fast. Our device prototype can compute incoming signal trains operating as pulse counter with resets occuring for different cycle periodicities, which are observed for the first time with a single nanoscale device, labeled as "super-cycles". This observation is explained in terms of *a nanoscale tipping bucket effect*. The capacitance-voltage response unveils that the structure shows a voltage-controlled hysteretic memcapacitance[8] with possible application as computing memory.[29,30] Thus, our findings may pave new ways to highly functional memcomputing networks, an appealing and interesting parallel computing approach, with a mature technological platform of site-controlled quantum dots.

Our device (see Figure 1 (a) for a scanning electron micrograph and experimental circuit diagram) consists of InAs quantum dots (QDs) positioned deterministically inside a transistor channel. For this purpose, laterally aligned InAs QDs were fabricated by site-controlled growth based on a patterned nanohole template via molecular beam epitaxy of a modulation-doped GaAs/AlGaAs heterostructure. Using electron beam lithography and etching techniques, a narrow channel with a minimum width of 120 nm and lateral side-

gates separated by 50 nm from the channel were defined. Description of typical fabrication techniques, including a QD accurate alignment procedure, can be found in Refs. 31 and 32. All measurements were performed in the dark by immersing the sample in liquid helium at $T = 4.2$ K. The diagram in Figure 1 (b) represents the expected memcapacitive $C - V_g$ curve as reported in Ref. 8 and the $C - V_g$ response of our device is plotted in Figure 1 (c) confirming it as a memcapacitor.

The floating-gate memory function of the QDC was studied by means of periodic gate voltage sweeps. The bias voltage, $V_b = 100$ mV, and the gate voltage, V_g, were applied to the drain and side-gates of the device, respectively. The source was grounded. Periodic closed gate voltage sweeps (cycles) were performed, going from V_{gs} up to V_{gm} (up-sweep) and back (down-sweep), at a constant sweep rate of $\nu = |\mathrm{d}V_g/\mathrm{d}t| = 0.2$ V/s (the voltage profile is shown in Figure 1 (a)). Figure 1 (d) shows the current-gate voltage (I-V_g) curves during seven consecutive gate cycles at $V_{gs} = -3.00$ V and $V_{gm} = 3.35$ V (left), and $V_{gm} = 3.70$ V (right). For $V_{gm} = 3.35$ V (Figure 1 (d), left), the channel opens at 1.27 V (up-sweep) and closes at 0.80 V (down-sweep), with a hysteresis width of about 0.47 V. Changing V_{gm} to 3.70 V leaves the up-sweep almost unaltered, but changes the hysteresis width to 2.1 V. A variation in the QDs charge causes the hysteresis.[33] In our QDC, QDs are charged at negative and discharged at positive gate voltages,[32] which is inverse to the behavior of top gate structures.[33–35] The inversion results from the implementation of lateral side gates and can be reinverted again by increasing the bias voltage, as shown in Ref. 36. In what follows, the smaller hysteresis loop is referred as S-cycle and the larger one as R-cycle (reset-cycle). The emergence of the R-cycle can be explained by a second discharging channel that opens at higher voltages.[32]

Our devices were subjected to multiple gate voltage sweeps, with V_{gm} ranging from 3.35 V to 3.70 V. At $V_{gm} = 3.35$ V, the I-V_g curves always have the shape of S-cycles, while we only observe R-cycles for $V_{gm} = 3.70$ V. At intermediate values of V_{gm}, a periodic alternation of R- and S-cycles was observed, with a super-period N^P. For example, Figure 2 (a) shows

seven consecutive cycles (bottom-up) measured at $V_{gm} = 3.60$ V (left) and $V_{gm} = 3.55$ V (right). One can clearly distinguish a period doubling ..-R-S-R-S-R-S-R-.. ($N^P = 2$) at $V_{gm} = 3.60$ V and period tripling ..-R-S-S-R-S-S-R-.. ($N^P = 3$) at $V_{gm} = 3.55$ V. Figure 2 (b) shows the variation in the occurrence probabilities of R-cycles and S-cycles with the maximum gate voltage. Each data point corresponds to the fraction of R- or S-cycles in 100 sweeps. One can observe well-defined plateaux at 0.5, 0.33, 0.25 and 0.20 fractions of R-cycles, corresponding to stable super-cycles with periods from two to five.

To investigate the physical origin of this tipping bucket effect we have experimentally measured the gate-to-channel capacitance-voltage curve of the QDC, which is shown in Figure 1 (c). As already stated, the capacitance is bistable and very similar to a model capacitance-voltage ($C - V_g$) curve of a threshold-type bipolar memcapacitive system[8] sketched in Figure 1 (b). The bistability in the $C - V_g$ curve originates from the changing quantum capacitance of the channel when charging the QDs. As the QDs become charged with electrons, the quantum capacitance-gate voltage-curve shifts towards larger gate voltages (see the Supplementary materials). The changing quantum capacitance alters the gate efficiency, which in turn is bistable and accounts for changes in the gate voltage to amend the charging and discharging energies.The memcapacitance C_M of the system thus affects the gate efficiency $\eta \propto C_M$ in a bistable manner, which in turn influences the QD charging and discharging (see the Supplementary materials) in such a way that supercycles of the reset occur. Information is thus not only stored in the QDs via localized charges, it can be also processed in the phase of the reset periods.

To model our observations we introduce a single continuous variable n_{dot} to represent the number of electrons on the central QD. n_{dot} plays the role of the internal state variable,[8] whose evolution is described by a phenomenological rate equation

$$\frac{\mathrm{d}n_{dot}}{\mathrm{d}t} = -\left[\frac{f(\Delta\epsilon_r)}{\tau_r} + \frac{f(\Delta\epsilon_d)}{\tau_d}\right] \cdot n_{dot} + \frac{f(-\Delta\epsilon_c)}{\tau_c}. \tag{1}$$

Here τ_i $(i = r, d, c)$ are the time constants for the reset, charging and discharging processes that are triggered by the energy differences $\Delta\epsilon_i = \alpha_i n_{dot} + \epsilon_i - \eta_i e V_g$, where ϵ_i is the threshold energy for process i. α_i, η_i account for the Coulomb interaction and gate efficiency, respectively, and e is the electron charge. Moreover, $f(\Delta\epsilon_i < 0) = 1$ and $f(\Delta\epsilon_i \geq 0) = \exp(-\Delta\epsilon_i/k_b T)$, k_b being the Boltzmann's constant, and T the temperature. The current through the channel is defined by n_{dot}, V_b, and V_g (see the Supplementary materials for details). The role of different terms in the right-hand-side of Eq. (1) is as follows. The first (r) term describes the discharging with short time constant (related to R-cycles) and the second (d) term discharging with larger time constant (S-cycles). The last (c) term corresponds to the QD charging and accounts for the programming operation of floating gate devices, i.e. electron tunneling onto the floating gate.[37] The tunneling rate depends on the tunneling distance and the potential barrier height. For the presented device, the large tunneling distance leads to large charging times in the order of 5 s.[32] Even larger times between 300 and 4000 s have been observed for quantum dot floating gate devices with tunneling distances of 40 nm.[38] The reset term on the other hand accounts for the discharging of the floating gate (erase operation), which takes place on time scales of $t_d \approx \mu s$. Moreover, the reset voltage (threshold voltage of the reset) of the device is found to be charge dependent.[39] In the simulation, the charge dependency of the reset process is accounted by a non-zero value of α_r ($\alpha_d = \alpha_c = 0$).

Results of our numerical simulations based on Eq. (1) are in a very good agreement with experimental observations. For example, Figure 2 (c) displays some numerical results clearly showing the alternation of S- and R-cycles similar with the reported experimental results. For obtaining a deeper understanding of our model, let us consider the localized charge dynamics. First of all, we note that there are two QD charge thresholds, n_c and $n_c - \Delta n$, where Δn is the width of the variation interval. In the super-cycle regime, after each charging to n_c, the QD is discharged, by several sweeps, down to $n_{dot} = n_c - \Delta n$ leading to a maximum number of S-cycles N^{max} before the QD is charged again.

To obtain analytically the limiting cases of the counting limits of our model, we note that there are two QD charge thresholds, n_c and $n_c - \Delta n$, where Δn is the width of the variation interval. Keeping only the discharge term in the right-hand-side of Eq. (1) and assuming $n_{dot}(t=0) = n_c$, one can find the maximum number of S-cycles such that $n_{dot}(t) > n_c - \Delta n$

$$N^{max} = \lfloor -\frac{\tau_d}{\Delta t_d} \ln\left(1 - \frac{\Delta n}{n_c}\right) \rfloor. \tag{2}$$

Here, the brackets $\lfloor\ \rfloor$ denote the floor value of a real number and $\Delta t_d = 2(V_{gm} - \epsilon_d)/\nu$ is the time spent while discharging. It follows from Eq. (2) that there are no or infinite S-cycles when $\Delta n/n_c \to 0$ or 1, respectively.

Next, we consider a sequence of S-cycles followed by an R-cycle, ruled by the two first terms in the right-hand-side of Eq. (1). The reset channel in Eq. (1) is modeled using $\alpha_r \neq 0$, $\eta_r = 1$, and $\tau_r << \tau_d$. Considering now only the two first terms in the right-hand-side of Eq. (1), one can find the number of S-cycles N_S before a reset

$$N^S = \begin{cases} \lfloor L(V_{gm}) \rfloor, L(V_{gm}) \geq 0 \\ 0, L(V_{gm}) < 0 \end{cases} \tag{3}$$

where $L(V_{gm}) = -\tau_d/\Delta t_d \ln[(V_{gm} - \epsilon_r)/(\alpha_r n_c)] + 1/2$.

Figure 2 (d) depicts N^{max} as a function of V_{gm} and $\Delta n/n_c$. N^{max} ranges from no to infinite S-cycles when $\Delta n/n_c \to 0$ or 1, respectively. These limiting cases define hypothetical counting limits of our model. One can find that the relative width of the memcapacitance bistability determines the condition for the occurrence of an R-cycle after N^S S-cycles. If $N^{max} > N^S$, the maximum number of S-cycles before reset is N^S, as shown by the contour plot in Figure 2 (d). Under this condition, one R-cycle will be triggered for every $N^P = N^S + 1$ applied voltage periods, so that its probability is given by $P = 1/N^P$ included as the fit in Figure 2 (b) and the dotted line in Figure 2 (e). Otherwise, our model predicts no R-cycles and, in the limit $(n_c - \Delta n) \to 0$, the counting range expands, in principle, to infinity.

The periodicity of the QDC response can be explained using an analogy with a tipping bucket as shown in Figure 3 for the period doubling. The 3D schemes illustrate the charge configurations in the QDs and the channel, and the current flow for two gate voltage sweeps. E.g. Figures 3(a) and (c) show the down-sweep cycles of an R- and S-cycle, respectively (the 3D scheme corresponds to the gate voltage marked with the red dot in the $I - V_g$ characteristic). The red spheres in 3D schemes represent electrons, whose distribution in the channel depends on the amount of localized charge. Charged quantum dots locally deplete the conduction channel. The depletion area is shown as gray shaded region and electrochemical potentials of the source and drain contacts are represented by the red and orange shaded regions. The center of Figure 3 displays the associated tipping bucket configuration. A tipping bucket tips (resets) as the water level exceeds a certain threshold. For continuous water flow into the bucket, the reset occurs periodically with a period determined by the ratio of the tipping bucket capacity and the amount of water added per unit time. The tipping bucket thus allows to determine the water flow by counting tipping events. In the presented device, the quantum dots behave as a bucket for electrons. Please note that in our analogy, the full bucket corresponds to the minimum amount of localized electrons. Removing electrons from the QDs by sweeping the gate voltage to positive values leads to more positively charged QDs (represents adding of water to the bucket) and a subsequent reduced Coulomb repulsion between the dots and the channel. As the amount of QDs charge is below a certain value, the threshold voltage V_d of the fast discharging process shifts below the maximum gate voltage ($V_d \propto n$),[39] the QDs become fully discharged, which triggers the charging when sweeping the gate voltage back to the minimum value. The bucket tips. Figure 3 (a) displays the configuration for discharged QDs and a large current (electrons in the channel below the QDs). At negative voltages, the QDs become fully charged (between Figures 3 (a) and (b)), which corresponds to the tipping of the bucket. For positive voltages (between Figures 3(b) and (c)), electrons are removed from the QD, making it more positively charged. This corresponds to adding positive charges (adding water to the tipping bucket). A critical value of QD charge

in Figure 3 (d) leads to an R-cycle and the consecutive charging of the QDs with electrons, just as the water level above a threshold tips the bucket. Thus adding an amount of charge (water) to the QDs (bucket) by several gate voltage sweeps, leads to the removing of all positive charges (tipping of the bucket). The dependency of the gate-channel-capacitance on the QD charge is sketched with varying distances between the gates and the channel (large distances for charged QDs correspond to a small capacitance).

To estimate the reproducibility of the super-cycles, the device was subjected to about 1000 cycles at V_{gm}. Figure 4 (a) shows the hysteresis width of 100 consecutive cycles for super-cycle periods 2, 3 and 4 (from top to bottom). The reproducibilities of R-cycles with periods $N^P = 2$ and 3 are high. However, there are few errors at $N^P = 4$, such as the occurrence of two or four S-cycles between consecutive R-cycles. Figure 4 (b) shows the experimentally and theoretically obtained reliability (top) and error probabilities (bottom) for super-cycle periods from 1 to 5. The reliability and the failure probability for the expected period N^P for any amount of missing or additional counts, $\Delta N^S = \pm 1, \pm 2, ...$, can be estimated unambiguously for a normal noise distribution with a given standard deviation, σ, that accounts for threshold voltage fluctuations. The 99 % reproducibility of the double period falls to 87%, 83 %, and 75 % for periods 3, 4 and 5, respectively. Figure 4 (c) shows theoretical reliability and error probabilities as functions of the maximum gate voltage for noise standard deviations of $\sigma = 5$, 10, and 15 mV. It is not surprising that the reproducibility is higher in the centers of the plateaux. The theoretical values in Figure 4 (b) were obtained with $\sigma = 10$ mV.

To summarize, we have demonstrated a QDC based on QD-charging bistability in a mem-capacitive structure showing remarkably reproducable capacitance and resistance switching. Samples with slightly different geometry and quantum dot position show similar response with slightly varying threshold voltages for charging and discharging processes, i.e. show super-cycles with maximum voltage-dependent periods. As capacitance bistabilities have been demonstrated for various floating gate devices,[40–44] we predict that, according to Eq.

(2), the super-cycling could be observable in many other non-volatile memory devices if the discharging time τ_d is large compared to the time spent in the discharging region of the gate voltage, Δt_d. To observe the cycling, a reset process (fast discharging) leading to a large and measureable conductance change is required. The QDC shows a complex functionality not available with a single CMOS device (e.g., a field-effect transistor). The nanoscale tipping bucket effect of the presented quantum dot transistor-based counter may be employed in multi-level logic applications for basic mathematical operations such as addition and subtraction. Additionally, we anticipate that this functionality could be of use in artificial neural networks, for example, as part of an integrate-and-fire neuron. Indeed, the pulse counting is similar to integration and the device reset could be associated with the neuron firing. Our study presents a general protocol for a compact pulse counting device, in which device-specific time scales, counts ranges and reliability can be adjusted via heterostructures device engineering. The low temperature operation described in this letter is a limitation that clearly reduces the applicability of the current QDC, although the desired room temperature operation can be tuned by energy scale engineering. Yet, the fundamental idea of combining dynamically different memcapacitive regimes as proposed here, can be a roadmap for quantum dot based architectures with inherent memory that require counting as a basic operation. Also, the practicality of memcapacitors and memristors in the context of neuromorphic[39] and/or arithmetic circuits[45,46] is an established fact where the impact of the current receipt could be expected. Our observations enable experimental implementation of logic and neuromorphic architectures, combining information processing and storage on the same physical platform.

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Supporting Information Available

The following files are available free of charge. Extended description of theoretical model, capacitance bistability of the gate-channel capacitance, theoretical count limits of the super-cycles and reset probability

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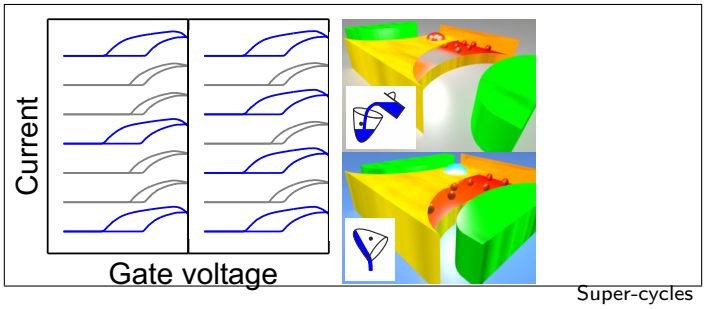
Graphical TOC Entry



Super-cycles under two different incoming signal trains and the nanoscopic tipping bucket scheme.

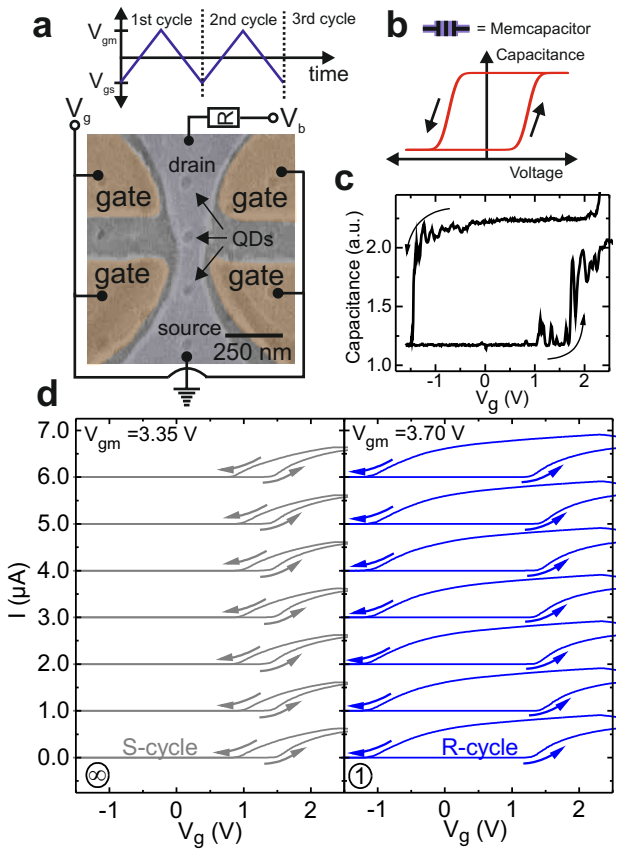


Figure 1: Memcapacitive quantum dot-based counter. (a) An electron microscope image of the device, electronic circuit diagram and gate voltage waveform. The device is composed of laterally aligned InAs QDs, a transistor channel and laterally defined side gates. The bias voltage, V_b, and the gate voltage, V_g, are applied to the drain and side-gates of the device, respectively. The source is connected to the common ground. Periodic closed gate voltage sweeps were performed by sweeping V_g from a starting value V_{gs} up to a maximum value V_{gm} and back at a constant sweep rate. (b) Schematic of a memcapacitor $C - V_g$ curve (see, e.g., Figure 4 in Ref. 8). (c) Experimentally measured $C - V_g$ curve of the quantum dot-based counter. (d) $I - V_g$ curves measured at $V_b = 100$ mV and $V_{gm} = 3.35$ V (left) and $V_{gm} = 3.70$ V (right). The curves related to consecutive sweeps were offset by 1 μA for clarity. While $V_{gm} = 3.35$ V results only in small hysteresis (S-cycles), $V_{gm} = 3.70$ V leads only to large ones (R-cycles). The circled numbers label the periodicity of R-cycles.

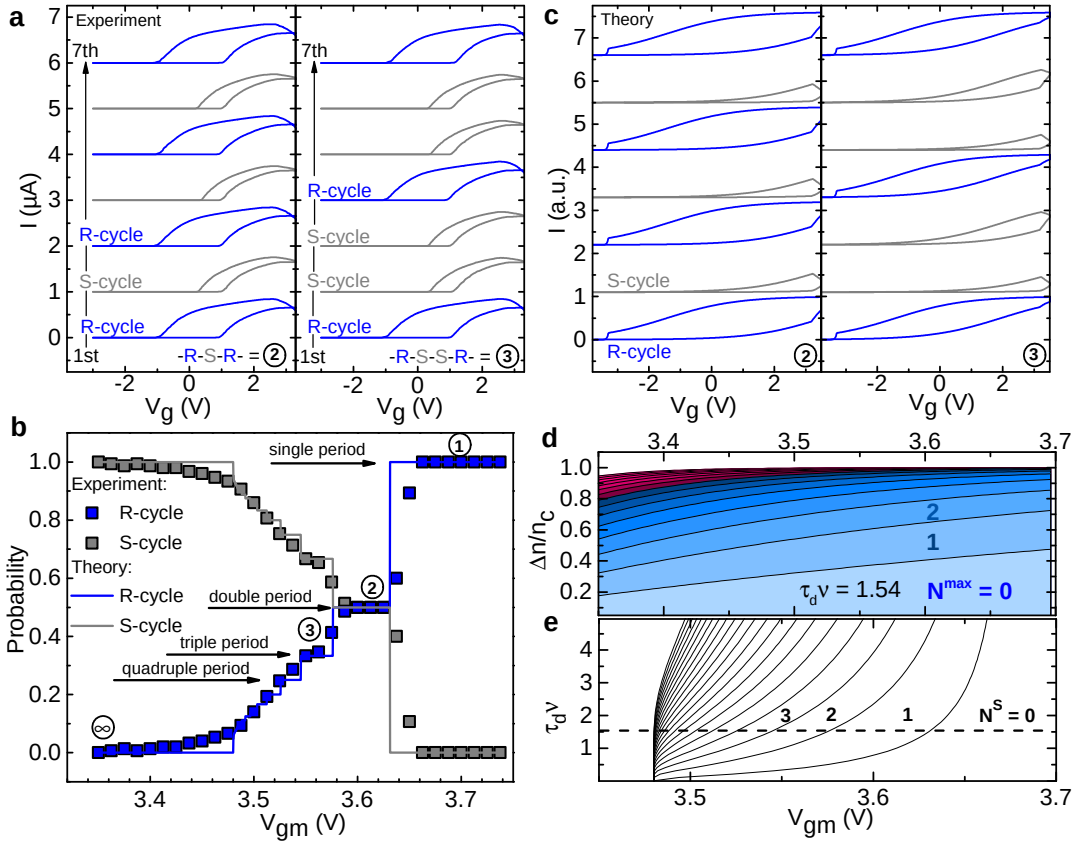


Figure 2: Super-cycles. (a) $I - V_g$ curves for seven consecutive gate sweeps at $V_{gm} = 3.60$ V (left) and $V_{gm} = 3.55$ V (right). At $V_{gm} = 3.60$ and 3.55 V, R-cycles occur every second and third gate period, respectively. The super-cycle period increases with decrease of V_{gm}. The curves for different gate sweeps are offset by 1 μA for clarity and organized bottom-up. (b) Experimentally (grey and blue filled squares) and numerically (solid lines) determined probabilities for R- and S-cycles as functions of V_{gm}. The probability of R-cycles decreases with decrease of V_{gm} below 3.66 V with well distinguished plateaux at 0.5, 0.33, 0.25 and 0.20. Each plateau corresponds to a stable super-cycle period. (c) Numerical modeling of super-cycles based on Eq. (1) model with $\Delta n/n_c = 0.8$. (d) The maximum number of S-cycles, N^{max}, before a charging event neglecting reset as a function of V_{gm} and $\Delta n/n_c$. (e) The number of S-cycles before reset, N^S, as a function of V_{gm} and $\tau_d\nu$. The dotted line corresponds to the parameters used to calculate the theoretical curves in the panel (b).

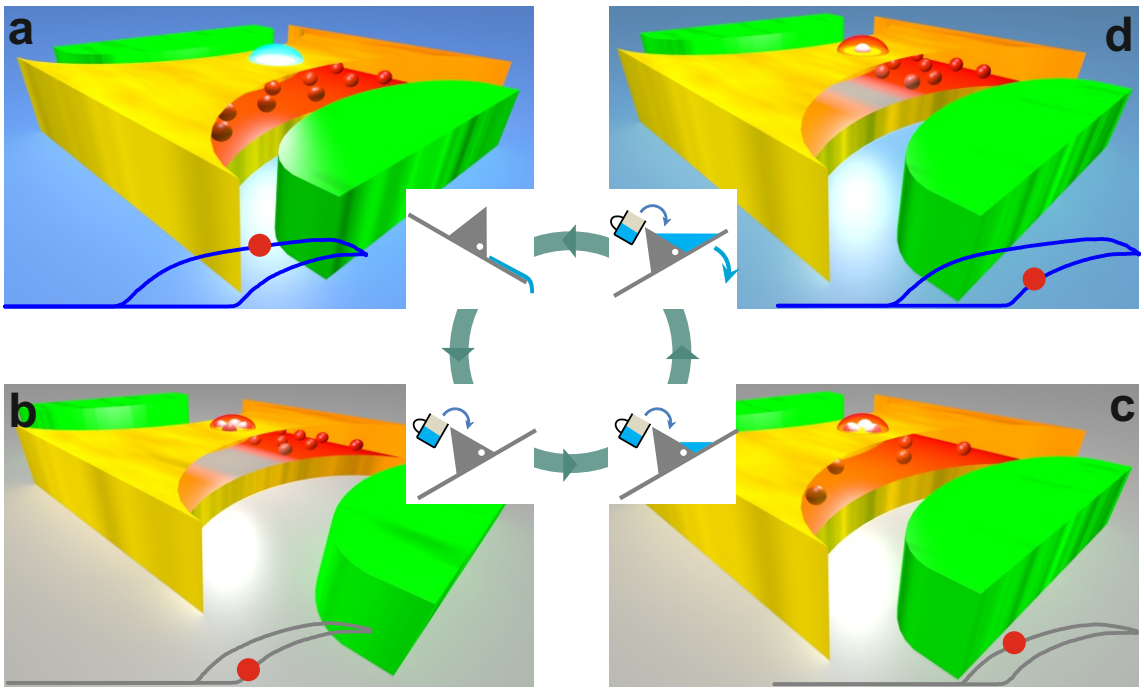


Figure 3: Tipping bucket model of super-cycle behavior. The tipping of a leaky bucket depends on the amount of water added periodically. Super cycles (such as the period doubling) are possible for an intermediate amount of water added. Initially, the QD is empty (in **a**) and becomes fully charged at negative voltage (from **a** to **b**). Each time a positive voltage is applied (from **b** to **d**), some electrons are removed from the QD, making it more positively charged. A critical value of QD charge (**d**) leads to an R-cycle, just as the water level above a threshold tips the bucket. The 3d plots show the QDC charge configuration and current (red dot in the I-V characteristic) for the period doubling.

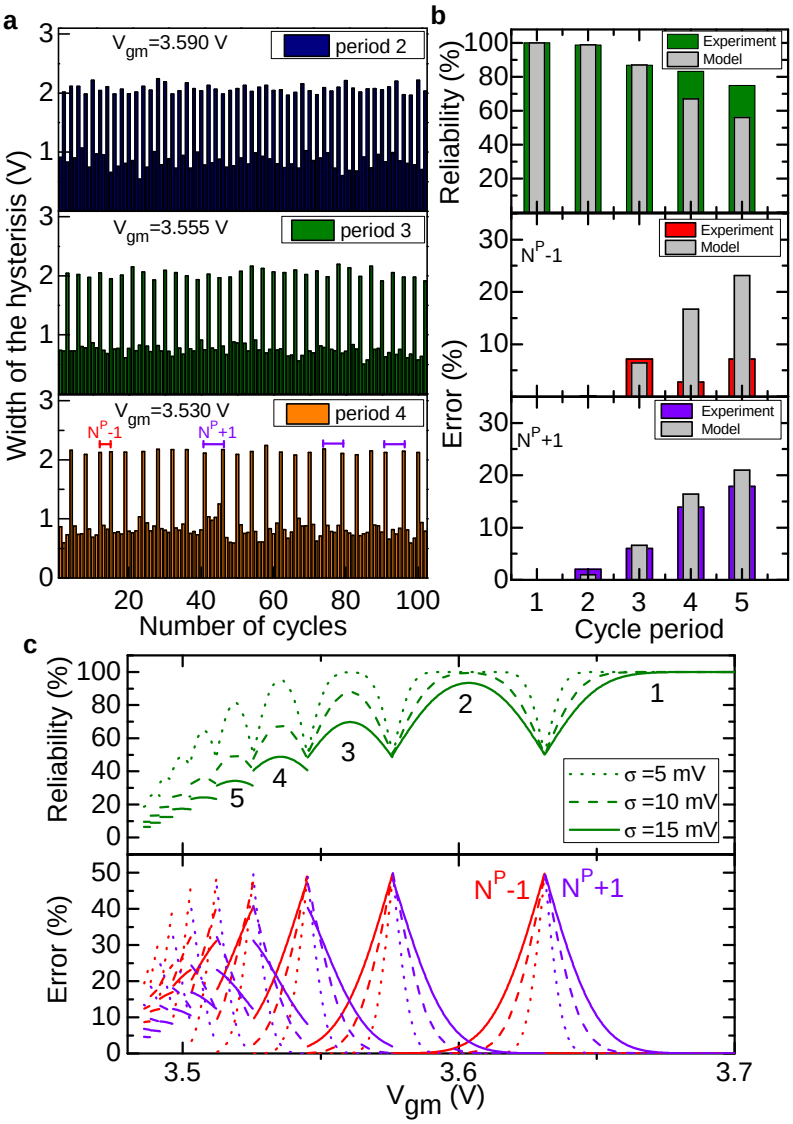


Figure 4: Reproducibility and error probability of super-cycles. (a) Hysteresis width for consecutive gate voltage sweeps for double, triple and quadruple super-periods. While super-cycles of smaller periods ($N^P = 2$ and 3) are highly stable, super-cycles of larger periods (such as $N^P = 4$) show a lower reproducibility with a possibility of $N^P - 1$ and $N^P + 1$ super-periods. (b) Experimentally and theoretically obtained reproducibilities (top) and error probabilities (bottom) of super-cycles with period N^P. The error probabilities describe deviations of super-periods from the expected value of N^P. (c) Calculated reproducibilities and error probabilities as functions of V_{gm} for noise standard deviations $\sigma = 5, 10$ and 15 mV. The theoretical values in (b) were obtained at $\sigma = 10$ mV using V_{gm} from the experiment.