

Associative learning with Y-shaped floating gate transistors operated in bistable modes

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We present Y-shaped three-terminal floating gate transistors with positioned quantum dots (QDs) acting as floating gates. The QDs are precisely positioned in the input terminals and the localized charge controls the conductance of the transistors. Connecting two devices enables to implement associative learning by tuning the QD-charge with two input signals. The number of pulses to develop or to forget the association depends on the widths and amplitudes of the applied voltage pulses. The Y-shaped geometry of the presented device may be considered to implement synaptic functionalities without separating learning and signal transmission in time.

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Associative learning in neural networks is crucial and required to relate new experience with existing memories and was first observed by I. Pavlov in his famous dog experiment.¹ Stimulating different senses by the sight of food and the sound of a bell, I. Pavlov trained his dog to correlate salivation with the sound of the bell (association), although at the beginning of the experiment salivation was only triggered by the sight of food. In neural networks, association corresponds to an increase of synaptic strength, which is controlled by action potentials emitted by pre- and postsynaptic neurons.^{2,3} Associative learning can be emulated with memristive Hopfield neural networks,⁴ memristive circuits^{5,6,7,8} or magnetic tunnel junctions.⁹ Other demonstrations of associative learning implement two artificial synapses with memristor emulators¹⁰ or a resistor and a memristor.¹¹ Artificial synapses based on memristors enable synaptic modifications by applying pre- and postsynaptic voltage pulses to the two terminals of the device,^{12,13} which allows to combine information storage and processing on the same physical platform.^{14,15,16} Owing to the two-terminal character, however, the application of postsynaptic voltage pulses blocks the device output and prevents information to be transferred during the learning process. The devices separate signal transmission and learning. Hence, three-^{17,18,19} or even four-terminal²⁰ synaptic devices may be beneficial because of their ability to decouple the postsynaptic pulse from the output. Indeed, associative learning with simultaneous learning and signal transmission has been demonstrated with three-terminal synapses based on nano-particle organic memory field effect transistors by applying postsynaptic pulses with amplitudes as large as 30 V to the third terminal.²¹ In memristor-synapses, extra terminals may be implemented with additional gates that allow tuning the set voltage with an electric field effect.²²

We report associative learning with Y-shaped quantum dot floating gate transistors operated in memristive modes. The geometry of the devices with two input terminals and one output terminal enables realizing associative learning with postsynaptic voltage amplitudes as low as 0.5 V. The

conductance of the Y-shaped quantum dot floating gate transistor depends on the amount of localized charges on quantum dots (QDs) that are precisely positioned in the two input terminals. Emulating external stimuli “food” and “bell” with two input voltages allows implementing an association between “bell” and “salivation”. The number of required pulses to develop (association) or to forget (extinction) the correlation between “bell” and “salivation” is controlled by the amplitudes of the input voltages.

Fig. 1(a) shows an electron microscopy image of the Y-shaped floating gate transistor. The device is based on a modulation doped GaAs/AlGaAs heterostructure and was grown by molecular beam epitaxy on a GaAs substrate. After a GaAs buffer and GaAs/Al_{0.2}Ga_{0.8}As superlattice layers, 2 μm undoped GaAs, 30 nm undoped Al_{0.2}Ga_{0.8}As, 50 nm n-doped (Si, $1 \times 10^{18} \text{ cm}^{-3}$) Al_{0.2}Ga_{0.8}As, and 10 nm undoped GaAs were grown. The electron waveguide, consisting of a stem (ST) that splits into a left (LB) and right branch (RB), was fabricated by electron beam lithography and dry chemical etching. QDs were precisely positioned in the two branches and at the branching section by growing InAs on a predefined pattern of 50 nm deep holes. The holes with diameters of 100 nm were realized by electron beam lithography and dry chemical etching (see Refs. 23, 24 for more insights in the fabrication process). The dark contrasts in Fig. 1(a) correspond to the positions of the QDs and the etched trenches that isolate the electron waveguide from the side gates. The positioning of QDs is described in Ref. 23. The presented measurements are conducted at 4.2 K in the dark.

Connecting the voltage applied to the drain contact (i.e. right branch V_r) with the side gates (see Fig. 1(a)) leads to a memristive operation.^{25,26,27} The Y-shaped floating gate transistor is characterized by applying the voltage $V_r = V_1$ to both branches with resistances of $R_l = R_r = 1 \text{ M}\Omega$ in series to the branches. The current-voltage-characteristics at the left, I_l , and the right branch, I_r , show pinched hysteresis loops as depicted in Fig. 1(b). The high and low conductance (on- and off-state) around zero

bias voltage correspond to discharged and charged QDs, respectively,²⁷ since the localized electrons reduce the mobility and the charge carrier density of the channel.²⁸ For the on-state (discharged QDs) and voltages between 4.8 and -1.0 V, I_r and I_l coincide. Thus the two branches have comparable resistances due to the left-right symmetry. As the QDs become charged (below -1.8 V), I_l and I_r differ, and the current in the left branch is smaller compared to the current in the right branch. Also, the onset of current flow for the left branch is observed at a larger voltage $V_{tu,l}$, i.e. $V_{tu,l} > V_{tu,r}$. Both observations correspond to larger amounts of QD localized charges.^{27,29} This indicates that the positioned QDs become charged independently in the two branches, since charged QDs localized in the branching or the stem section would affect the currents in both branches equally. Hence, the QDs in the two branches are charged independently leading to different amounts of localized charges and to current-voltage-asymmetries between the left and the right branch in the off-state. Discharging of the QDs is observed for $V_d \approx 3.7$ V. The required amount of electrons to control the conductance depends on the effective capacitive coupling between the gates, the QDs and the channel.³⁰ Realizing the channel with similar dimensions as a single QD may allow the observation of single electron charging and discharging events, as demonstrated with the floating gate transistor in Ref. 30.

Fig. 2(a) displays I_r - V_r -characteristics for constant voltages V_l applied to the left branch. The sweep is performed with V_r applied to the right branch and the two side gates. For non-zero values of V_l the hysteresis is off-centered and shows a linear shift with slope 0.6, as indicated by the brown arrow in Fig. 2(a). Depending on V_l , the voltage difference between the left and right branch differs and hence, I_r depends on V_l due to an effective voltage difference between the right branch and the branching section. In addition, V_l causes a shift of the discharging voltage V_d and a width variation of the low conductance plateau V_{th} (see Fig. 2(b)). An almost linear V_d - V_l -dependency with slope 1.6 is observed (as shown in Fig. 2(b)) that is caused by the effective channel-gate voltage difference in the right branch, which

depends on V_1 and allows larger amounts of charges to be accumulated for positive V_1 . The increasing number of charges on the QDs leads to larger V_{th} as well.²⁷ As shown in Fig. 2(b), V_{th} only increases for negative V_1 (slope: 2.6) but decreases for positive V_1 (slope: -0.3). The two slopes of the V_{th} - V_1 dependency can be explained by different threshold voltages of the three terminals as shown in Fig. 2(c). The largest threshold voltage is observed either for the stem (negative V_1) or the left branch (positive V_1). Thus for $V_r = V_{tu,r}$, the current flows either between the branches (negative V_1) or between the right branch and the stem (positive V_1) as indicated by the red arrows in Fig. 2(d). The other terminal (stem or left branch) is decoupled due to a depletion of the 2DEG and can act as an additional gate.^{31,32} Since the stem is connected to the common ground, no gating effect occurs for negative V_1 and V_{th} is proportional to V_d as reported in Ref. 27. For positive V_1 , the self-gating is opposed to the increase of V_{th} due to the increasing amount of localized charges leading to a decreasing width.

Fig. 3(a) sketches the network consisting of two Y-shaped quantum dot floating gate transistors Y_1 and Y_2 . The devices represent artificial synapses that connect two presynaptic neurons with one postsynaptic neuron (see Fig. 3(b)). Neuron functionalities are mimicked with function generators and the output voltages $V_{1,1}$ and $V_{r,2}$ (presynaptic neurons) and $V_{1,2}$ (postsynaptic neuron). Rectangular voltage signals $V_{1,1}$ and $V_{r,2}$ emulate the external stimuli “food” and “bell”, respectively. The conductance states of the devices represent the association between “food” and “salivation” (Y_1) and “bell” and “salivation” (Y_2). Y_1 and Y_2 are connected via a voltage amplifier and a function generator as threshold device to emulate postsynaptic neuron functionality. The function generator is triggered by the output of Y_1 for a 1 M Ω load. The generation of the voltage pulse corresponds to “salivation”. The signal $V_{1,1}$ (corresponds to “food”) triggers the function generator and releases a rectangular postsynaptic voltage pulse $V_{1,2}$ with amplitude -0.5 V (corresponds to “salivation”) for discharged QDs in Y_1 (see Fig. 3(c)). For charged

QDs the function generator is not triggered due to a larger voltage drop across Y_1 . Hence, $V_{1,2}$ is constantly zero (see Fig. 3(d)) which corresponds to no association between “food” and “salivation”.

Associative learning is investigated with the network presented in Fig. 3(a) and the pulses shown in Fig. 4(a). The pulse $V_{1,1}$ with amplitude 0.4 V represents the external stimuli “food”. The pulses $V_{r,2}$ with maximum 4.0 V and minimum -3.6 V correspond to “bell”. The large absolute voltages of $V_{r,2}$ are required to alter the amount of QD-localized charge by exceeding either the charging or the discharging voltage that are in the order of several volts. In principle the same amplitudes can be used to emulate the stimuli “food”, but 0.4 V are already sufficient to trigger the release of a postsynaptic pulse. The conductance state of Y_2 determines the association between “bell” and “salivation” and is measured via the current flow when applying a read-out pulse. Large and low currents represent strong and no association, respectively. Fig. 4(b) displays the current in Y_2 for the pulse sequence sketched in Fig. 4(a). The signal representing “food” is only applied for $N = 2$ and 9 (vertical red lines), while the “bell” signal is active for all pulses. Simultaneously exciting the network with both input signals increases the current, which corresponds to the development of association between “bell” and “salivation”. Only applying the “bell” signal lowers the current and emulates extinction.

The development of association with a single pulse in Fig. 4(b) is not practical and it would be desirable to control the number of pulses. To investigate varying pulse numbers, the width of the input signals and the amplitude of $V_{r,2}$ are varied in Figs. 4(c) and (d), respectively. In both figures, the “bell” and “food” signals are active during all pulses with $N > 0$. Varying the width or the voltage allows to tune the number of pulses to develop association (to increase the current) from a few to several hundred pulses.

Extinction was investigated in more detail for varying minimum voltages of the “bell” signal (see Fig. 5(a)). For $N = 1$, association is developed by simultaneously applying “bell” and “food” signals. For the following pulses ($N > 1$), only the “bell” signal is active ($V_{1,1}$ is zero). The current reduction, which corresponds to extinction, can be controlled with the minimum voltage. Fig. 5(b) depicts the current after 1, 3, 5 and 15 pulses versus the minimum voltage. For a minimum of -3.87 V the current drops to zero after the first pulse. Larger minimum voltages require more pulses to lower the current to zero and hence to forget the association.

Associative learning can also be implemented with two-terminal memristor synapses.¹⁰ The main advantage of using three terminal devices is the suitability for simultaneous learning and signal transmission.¹⁸ While information propagates from one input to the output terminal (i.e. from RB to ST in Y_2), a voltage applied to the second input terminal (LB in Y_2) allows inducing learning processes. **The three-terminal synapse based on a Y-shaped electron waveguide enables** implementing associative learning with absolute postsynaptic voltage amplitudes as low as 0.5 V (e.g. 30 V were used for the three-terminal synapse in Ref. 21). **Due to the low localization energies of the electrons (around 0.4 eV), the presented network does not operate at room temperature, but electron localization was observed up to temperatures of 165 K.²⁹ Larger operation temperatures may be realized with other III-V-semiconductor materials that show higher localization energies (e.g. GaSb and AlAs, see Ref. 33).**

In conclusion, we present Y-shaped quantum dot floating gate transistors suitable for associative learning. In a network consisting of two devices, association is implemented by connecting the output of one to an input terminal of a second device. Tuning the widths and amplitudes of the input signals controls the number of pulses to develop or to forget the association. The proposed three terminal geometry enables operation as artificial synapses without separating learning processes and information

transmission in time. The low temperature operation hinders direct applications of the device, but the present work lays the foundation for possible room temperature operation of associative learning in other material systems like GaSb/AlAs quantum dots that show larger localization energies.³³

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Figure captions:

FIG. 1. (a) Electron microscopy image of the device with its Y-shaped channel (yellow) and the side gates (red and blue). The dark contrasts indicate the positions of the QDs and the etched trenches. The bias voltages V_1 and V_r are applied to the left (LB) and right branch (RB), respectively. In addition, V_r is simultaneously applied to the left side gates (blue). The stem (ST) is connected to the common ground. (b) Current-voltage-characteristics obtained by simultaneously applying the voltage V_r to both branches and the left side gates. Pinched hysteresis loops are observed.

FIG. 2. (a) I_r - V_r -curves for different constant voltages applied to the left branch. For increasing V_1 , the discharging voltage V_d shifts towards larger values. The curves are offset by 2 μ A for clarity. (b) V_{th} and V_d as a function of V_1 . V_{th} increases for negative and decreases for positive V_1 . V_d shifts linearly with slope 1.6. (c) Threshold voltages of the three terminals versus V_1 . For positive and negative V_1 , the left branch and the stem show the largest threshold voltages, respectively, leading to current flow between the right branch and the stem ($V_1 > 0$) or between the two branches ($V_1 < 0$). (d) Schemes of current flow (red) and capacitive coupling (orange) for $V_r = V_{tu,r}$ and $V_1 = -0.5$ (left) and $+0.5$ V (right). For negative (positive) V_1 , the current onset is observed between the two branches (between the right branch and the stem).

FIG. 3. (a) Circuit diagram used to investigate associative learning. The Y-shaped quantum dot floating gate transistors Y_1 and Y_2 represent two artificial synapses. Connecting the output of Y_1 with an input of Y_2 via a function generator allows to control the state of Y_2 by $V_{1,1}$ and $V_{r,2}$. (b) Illustration of the pre- and postsynaptic neurons that are connected via the artificial synapses Y_1 and Y_2 . (c) Time trace of the input voltage of Y_1 (food) and the output of the function generator (postsynaptic voltage) for discharged QDs in Y_1 . Every incoming pulse triggers the release of a voltage pulse with negative amplitude, which corresponds to an association between “food” and “salivation”. For charged QDs the association is suppressed (see panel (d)).

FIG. 4. (a) Schematic time trace of the voltage signals used to demonstrate associative learning. The pulses $V_{r,2}$ (green) and $V_{1,1}$ (orange) correspond to the stimuli “bell” and “food”, respectively. (b) Current of Y_2 for the pulses sketched in panel (a). Applying “food” and “bell” signals simultaneously (vertical red lines) increases the current (development of association). (c) Current versus pulse number for different widths of the voltage pulses representing the signals “food” ($V_{1,1}$) and “bell” ($V_{r,2}$). Both signals are active for all pulses. Less pulses are required to raise the current for larger widths (corresponds to association). (d) Current versus N for different maximum values of $V_{r,2}$ and a constant width of 50 ms. For smaller maximum voltages, association is developed after more pulses.

FIG. 5. (a) Current of Y_2 versus pulse number. For $N = 1$ association is developed by simultaneously applying “bell” and “food” signals. During the following pulses, only “bell” is active ($V_{1,1}$ is zero). For smaller minimum values of $V_{r,2}$, less pulses are required to reduce the current to zero (corresponds to extinction). (b) Current of the data shown in panel (a) after the 1st, 3rd, 5th and 15th pulse versus

minimum value of $V_{r,2}$. The number of pulses to forget the association depends on the minimum amplitude of the signal representing “bell”.

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