An electro-photo-sensitive memristor for neuromorphic and arithmetic computing

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We present optically and electrically tunable conductance modifications of a site-controlled quantum dot memristor. The conductance of the device is tuned by electron localization on a quantum dot. The control of the conductance with voltage and low power light pulses enables applications in neuromorphic and arithmetic computing. As in neural networks, applying pre- and post-synaptic voltage pulses to the memristor allows to increase (potentiation) or decrease (depression) the conductance by tuning the time difference between the electrical pulses. Exploiting state-dependent thresholds for potentiation and depression, we were able to demonstrate a memory-dependent induction of learning. The discharging of the quantum dot can further be induced by low power light pulses in the nW-range. In combination with the state-dependent threshold voltage for discharging, this enables applications as generic building blocks to perform arithmetic operations in bases ranging from binary to decimal with low power optical excitation. Our findings allow the realization of optoelectronic memristor-based synapses in artificial neural networks with a memory-dependent induction of learning and enhanced functionality by performing arithmetic operations.

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I. INTRODUCTION

In the human brain the interconnection of neurons via synapses results in a massively parallel computational network [1]. Synapses, the connections between neurons, are constantly formed or eliminated [2, 3] and learning is associated with the modification of their strength that regulates the transmission of action potentials [4]. This modification is controlled by the superposition of action potentials generated by pre- and post-synaptic neurons. According to the model of spike-timing-dependent plasticity (STDP), the relative timing of pre- and post-synaptic spikes is crucial for dynamic potentiation or depression [5–8]. In neural networks, neuronal activities do not necessarily result in changes of synaptic strength, but also in a varying capability for the induction of potentiation or depression [9, 10], which ensures intrinsic convergence of synaptic strength [11]. Recently, STDP was demonstrated with memristors [12–15] and interconnecting memristors with neurons, STDP-based learning rules can be emulated in self-learning visual cortices [16]. The memory resistance (memristance) of memristors [17, 18] can originate from different physical mechanisms such as self-heating, chemical reactions, ionic transfer, spin polarization or phase transitions [19]. In addition, a memristive operation mode was observed for floating gate transistors wired as diode connected transistors [20, 21]. Floating gate transistors are non-volatile memories based on field-effect transistors that store information by means of localized charge on an additional gate located between the channel and the control gate [22, 23]. Silicon-based floating gate transistors are used in commercially available non-volatile flash memory devices such as USB memory sticks and solid state hard drives. Current Si-based devices with feature sizes of 20 nm show room temperature retention times of more than ten years, and write and access times of about 1 μs and 10 ns, respectively [24]. Novel approaches in the design of these memory devices e.g., a three dimensional layout similar to the Tri-gate transistor, further tend to push their feature size limits and thus aims to keep track with Moore's law [25]. However, silicon is an indirect band gap semiconductor, which makes it impracticable for optical applications. Thus device concepts based on low dimensional direct bandgap semiconductors are especially appealing for an optical and electrical control of charge or spin states. Here quantum dot structures based on III-V-semiconductor materials with their atom-like energetic structure in combination with a direct band gap enable optoelectronic applications such as lasers [26], single photon sources [27], entangled-light-emitting diodes [28], spin memories [29, 30] and floating gate transistors [31]. Realizing STDP on a state-of-the-art opto-electronic semiconductor platform would thus allow the realization of electro-photo-sensitive artificial synapses and brain-inspired computing with optical interconnects.

Here we present an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic computing. The conductance of the device emerges from different amounts of quantum dot (QD) localized charges which can be controlled and altered by electrical and low power optical pulses. Applying nature-inspired voltage pulses to emulate the action potentials of pre- and post-synaptic neurons, the conductance of the device is raised (potentiation) or lowered (depression) by changing the time difference between the onsets of the pulses. We

further observe a dependence of the conductance change on the initial state, which was set by the past biasing procedure. Thus previous input pulses are memorized and the capability for the induction of learning changes accordingly. Finally, we demonstrate an optical control of the memristance. Combining the optical tunability with the state-dependent threshold for potentiation, the device is a basic component for the realization of arithmetic operations with low power optical pulses.

II. DEVICE LAYOUT

Fig. 1(a) shows a scheme of the device, which is based on a GaAs/AlGaAs heterostructure with precisely positioned InAs QDs (highlighted in green). The fabrication process is described in detail in Ref. [32]. The memristive operation is realized by short-circuiting the source with the gate contacts (see Fig. 1(b))[20, 21]. This wiring scheme is known as diode connected transistor and can for example be used as temperature sensor [33]. In our case the transistor is a quantum dot floating gate transistor. In analogy to synapses in neural networks, where the plasticity is controlled by the action potentials of pre- and post-synaptic neurons, we apply two independent voltage pulses labelled as pre- and post-synaptic pulses to the two terminals of the device. The voltages V_{pr} and V_{po} are applied to the source and drain contacts, respectively (see Fig. 1(b)). The current I was measured as voltage drop across a resistor with $R = 1$ MΩ in series to the channel. All measurements were conducted at 4.2 K.

III. MEMRISTOR CHARACTERISTICS

Fig. 1(c) depicts the current-voltage-characteristic of the device. A closed voltage sweep of the voltage applied to the source and gate contacts between −3.8 and 4.6 V shows a pinched hysteresis loop, the fingerprint of memristors [34]. The low and high conductance values between −1 and 1 V are explained by different amounts of QD-localized electrons n with more charges corresponding to the smaller conductance. V_{th} is the width of the plateau with almost zero conductance and is linear dependent on the amount of localized electrons [21]. The QD becomes charged for voltages below $V_{\mathrm{c}} \approx -1.9$ V ($\Delta n > 0$) and discharged above $V_{\mathrm{d}} \approx 4.4$ V ($\Delta n < 0$). In Fig. 1(c), V_{c} and V_{d} are highlighted with the red vertical lines. Hence the conductance of the device is altered by changing the amount of QD-localized charges which depends sensitively on the time and the voltage value spent above the discharging or below the charging voltage.

The pinched hysteresis loop can be analysed by the width V_{th} of the plateau with almost zero conductance [21]. Fig. 1(d) displays the discharging voltage in dependence on V_{th}. V_{th} was increased by reducing the minimum bias voltage during the voltage sweep cycle in Fig. 1(c). Lower minimum voltages lead to more localized electrons and enhanced V_{th} [21]. A linear increase of V_{d} is observed for raising V_{th}. Strukov et al. explained the dependency of the threshold voltage on the state of the memristor with non-linearities in ion movements [35]. Here we describe the shift of the discharging voltage by means of a charge-dependent gate efficiency. Charging the QD with electrons lowers the gate-channel-capacitance. The quantum dot charge dependent gate-channel-capacitance emerges from the depletion of the channel via localized electrons on the quantum dot which effectively leads to a variable effective gate-channel distance with different charge accumulation interfaces. Thus discharging the QD leads to larger capacitances. Controlling the amount of localized charge with the lateral gates, a hysteresis in the capacitance-voltage-curve is evident, which is the fingerprint of memcapacitors [19, 36]. For reduced capacitances, larger absolute gate voltages are required to shift the potentials of the QD and the two-dimensional electron gas by the same energy. Thus the charging and discharging voltages are reduced and increased, respectively.

For excitation with constant parameters (voltage range, sweep time), the pinched hysteresis loop as well as the threshold voltages V_{d} and V_{c} are highly reliable

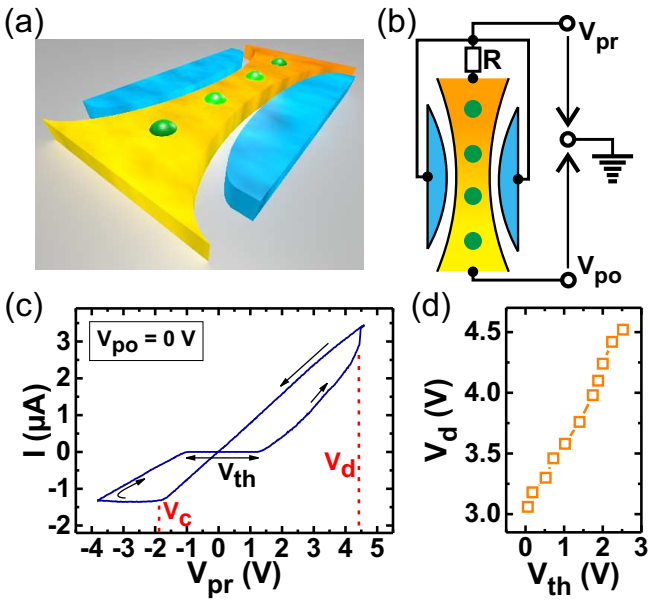

FIG. 1. **(a)** Scheme of the memristor. The positions of the QDs are highlighted in green. **(b)** Circuit diagram of the memristor. V_{pr} is applied to the top contact of the wire and the lateral gates. V_{po} is applied to the bottom contact of the wire. **(c)** Current-voltage-characteristic of the device. V_{c} and V_{d} are the threshold voltages for charging and discharging, respectively. **(d)** Linear dependency between the discharging voltage and V_{th}.

even after many voltage and temperature cycles with small deviations in the threshold voltages for charging and discharging in the order of 50 mV. The energy barrier height surrounding the floating gate, around 0.4 eV for the presented device, is significant lower compared to silicon-based floating gate transistors (3.2 eV) which leads to small retention times of several days at 4.2 K and stable pinched hysteresis loops up to temperatures of about 165 K [21]. Room temperature operation may be possible by tuning the material composition of the III-V compound semiconductors representing the QD and the surrounding matrix [31]. On the other hand, the reduced barrier height enables faster write and erase times and smaller operation voltages. A particular advantage of III-V-semiconductor-based compared to Si-based floating gate devices is the tunability of the energy barrier by changing the material composition. This may enable the realization of fast write times and room temperature retention times comparable to Si-based devices [31].

IV. SPIKE-TIMING-DEPENDENT PLASTICITY

Two function generators were used to emulate the voltage pulses in Fig. 2(a), that were applied to the two terminals of the device (see Fig. 1(b)). The general shape of the pulses was chosen to mimic an action potential measured in the axon of a squid [37]. Simple rectangular pulses are not used, because they only enable to either emulate potentiation or depression with a single set of pulses [21]. However, the transition from potentiation to depression solely triggered by the timing of the pulses is essential to mimic STDP and requires pulse shapes with positive and negative amplitudes. These pulse shapes allow to change the voltage difference across the memristor from negative to positive by inverting the temporal order of the two pulses. Thus charging or discharging of the QD can be induced depending on the order of the pulses. Because of the asymmetric charging and discharging voltages of the device, at least one pulse needs to be asymmetric. Thus we used amplitudes of $(+4.2, -3.1)$ and $(+2.0, -2.0)$ V for V_{pr} and V_{po}, respectively. The pulse widths were 10 ms. The time difference Δt between the pulses is the crucial parameter of STDP. Here, the post-synaptic pulse is applied after the pre-synaptic pulse for positive time differences and vice versa.

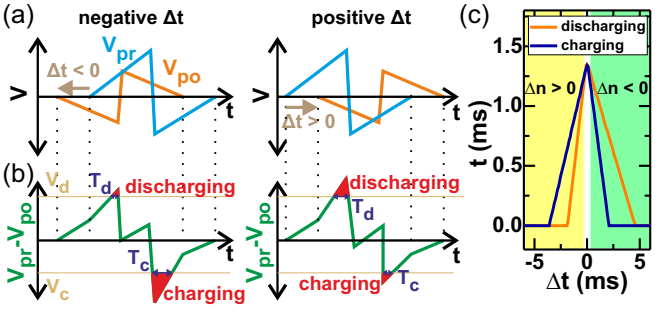

FIG. 2. **(a)** Scheme of pulse trains for negative (left) and positive (right) time differences Δt. The different voltages were applied to the two terminals of the memristor. Depending on Δt, $V_{\mathrm{pr}} - V_{\mathrm{po}}$ can exceed V_{c} and V_{d} (highlighted in red in (b)). The time intervals in the charging and discharging regions versus Δt are shown schematically in **(c)**. For positive and negative time differences, the QD is discharged (green area) and charged (yellow area), respectively.

For the present device, the performance is mainly governed by the voltage difference $V_{\mathrm{pr}} - V_{\mathrm{po}}$ between the two terminals. Depending on Δt, the temporal voltage difference can exceed the threshold voltages for charging and discharging (see red highlighted areas in Fig. 2(b)) for their respective times T_{c} and T_{d}. These time intervals depend on Δt, i.e. $T_{\mathrm{c}}(\Delta t)$ and $T_{\mathrm{d}}(\Delta t)$, as sketched in Fig. 2(c). For simple rectangular pulses, either T_{c} or T_{d} would be zero and independent on Δt. Thus tuning the time difference does not allow the observation of a transition from depression to potentiation. For the pulses in Fig. 2(a), the dominant processes are charging (highlighted in yellow) for negative and discharging (highlighted in green) for positive time differences. The time dependent tunneling from the two-dimensional electron gas to the QD (charging) and from the QD to the two-dimensional electron gas (discharging) can be described by a capacitor model [38]. The dependency of n on T_{c} and T_{d} is given by

$$n(\Delta t) = n_0 + n_+ \left\{1 - \exp\left[\frac{-T_c(\Delta t)}{\tau_c}\right]\right\} - n_- \left\{1 - \exp\left[\frac{-T_d(\Delta t)}{\tau_d}\right]\right\}. \quad (1)$$

n_0 is the initial amount of QD-localized charges. The second and third term of equation (1) represent charging and discharging characteristics with time constants τ_{c} and τ_{d}, respectively. n_+ and n_- are constants that represent the total amount of transferred charges.

Fig. 3(a) shows the conductance of the memristor versus the number of applied pulses N for different Δt. Here, one pulse is defined as pair of the pulses depicted in Fig. 2(a). Ten consecutive pulses were applied for constant time differences. Each pulse is followed by a read-out pulse with amplitude 2.8 V and width 5 ms to determine the conductance G. For large time differences (± 5.3 ms), the conductance remains almost unaltered up to ten pulses. Smaller time differences lead to an increase and decrease of the conductance with N for $+0.7$ and -0.7 ms, respectively. These observations are due to changes in the voltage difference across the memristor as a function of Δt. Varying time differences lead to different time intervals $T_{\mathrm{c}}(\Delta t)$ and $T_{\mathrm{d}}(\Delta t)$. For $\Delta t = \pm 5.3$ ms, they are almost zero and thus $T_{\mathrm{d}}/\tau_{\mathrm{d}} \approx 0$ and $T_{\mathrm{c}}/\tau_{\mathrm{c}} \approx 0$. Consequently the amount of QD-localized charges in equation (1) remains unaltered with $n(\Delta t) \approx n_0$ and

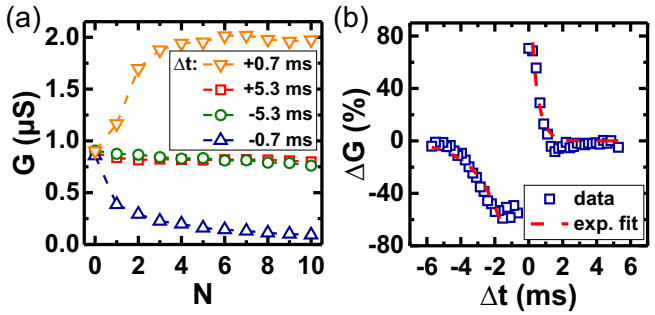

FIG. 3. **(a)** Conductance versus number of applied pulses for different Δt. G remains almost unaltered for large time differences ($\Delta t = \pm 5.3$ ms), but decreases and increases for $\Delta t = -0.7$ and $+0.7$ ms, respectively. **(b)** Relative conductance change versus Δt. In the interval of $\Delta t = \pm 4$ ms, ΔG can be tuned efficiently and either depressed or potentiated depending on the sign of Δt.

$\Delta n \approx 0$. For $\Delta t = \pm 0.7$ ms, the temporal signal exceeds the threshold voltages for times T_c and T_d greater than zero (see Fig. 2(c)). For negative Δt, the charging dominates over the discharging process with $T_\mathrm{c}/\tau_\mathrm{c} > T_\mathrm{d}/\tau_\mathrm{d}$, and the QD becomes charged with additional electrons (see equation (1)). Discharging the QD dominates for positive time differences.

To explain the influence of the amount of QD-localized charges on the conductance, we use the current-voltage-characteristic of a floating gate transistor

$$I = \beta \left(V_g - V_{tu}\right) V_b - \beta \frac{V_b^2}{2} \qquad (2)$$

with V_g and V_b being the gate and bias voltages, respectively, V_tu the threshold voltage and β the transconductance [20]. Charging the floating gate (here: QD) with electrons shifts V_tu of the nearby transistor with $V_\mathrm{tu} = ne/C$ (e: elementary charge, C: QD-gate-capacitance) towards larger values [39]. Additionally the carrier density and the conductance of the transistor are reduced for larger n [40]. In the memristive operation mode we have $V_\mathrm{g} = V_\mathrm{pr}$ and $V_\mathrm{b} \leq V_\mathrm{pr}$. Hence the second term in equation (2) can be neglected. With $V_\mathrm{tu} = ne/C$ it follows that the conductance $G = I/V_\mathrm{b} \propto ne/C$ is linearly dependent on the amount of QD-localized charges which in turn can be altered by the times spent in the charging and discharging regions (see equation (1)). Applying N consecutive pulses, the conductance change is

$$G_N(\Delta t) - G_0 \propto -n_+ \left\{1 - \exp\left[\frac{-NT_c(\Delta t)}{\tau_c}\right]\right\} + n_- \left\{1 - \exp\left[\frac{-NT_d(\Delta t)}{\tau_d}\right]\right\}. \qquad (3)$$

G_0 is the initial conductance and G_N is the conductance after applying N pulses. For negative and positive time differences we have $T_\mathrm{c}(\Delta t)/\tau_\mathrm{c} > T_\mathrm{d}(\Delta t)/\tau_\mathrm{d}$ and $T_\mathrm{c}(\Delta t)/\tau_\mathrm{c} < T_\mathrm{d}(\Delta t)/\tau_\mathrm{d}$, respectively. Thus for a given time difference, one term is negligible leading to the exponential decline of $G_\mathrm{N} - G_0$ for $\Delta t = -0.7$ ms and the exponential increase for $\Delta t = +0.7$ ms (see Fig. 3(a)).

Fig. 3(b) shows the relative conductance change after a single pulse $\Delta G = (G_1 - G_0)/G_0$ versus Δt. For each measurement, G_0 was set to 0.8 μS prior to the first pulse (see Fig. 3(a)). The relative conductance change depends exponentially on the time difference and can be tuned efficiently within a time interval of about 4 ms. Thus the relative conductance change is zero for large magnitudes of the time difference. The experimental data for positive and negative time differences can be fitted with single exponential fit functions $A \cdot \exp(\Delta t/\tau)$ (see equation (3)). The parameters are $A = 130$ % and $\tau = -0.4$ ms for positive and $A = 175$ % and $\tau = 1.6$ ms for negative time differences. The different time constants for charging and discharging (see Ref. [38]) result in a broader time window for depression than for potentiation.

V. STATE-DEPENDENT PLASTICITY

The conductance change of the memristor depends not only on the timing of the voltage pulses, but also on the initial conductance value G_0 as shown in Fig. 4. Figs. 4(a) and (b) illustrate the conductance versus N for various G_0 and time differences of $+0.9$ and -1.1 ms, respectively. The amplitudes of the voltage pulses were

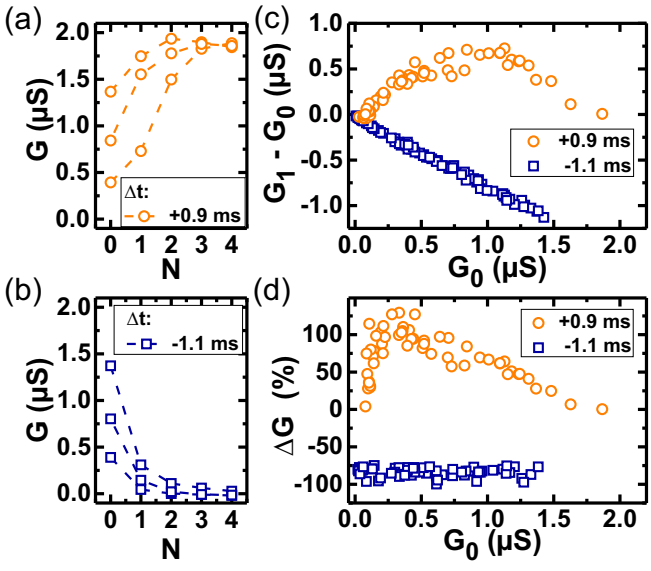

FIG. 4. **(a)** G versus N for different initial conductance values G_0 and time difference of $+0.9$. **(b)** Conductance versus pulse number for different G_0 and $\Delta t = -1.1$ ms. **(c)** $G_1 - G_0$ for potentiation ($\Delta t = +0.9$ ms) and depression ($\Delta t = 1.1$ ms). $G_1 - G_0$ decreases linearly for depression and shows a maximum for potentiation. **(d)** Relative conductance change versus G_0. ΔG is independent on G_0 for depression but can be modified over a large range for potentiation.

$(+4.2, -2.8)$ V for V_{pr} and $(+2.0, -2.0)$ V for V_{po}. Again, the conductance increases and decreases for positive and negative time differences, respectively. Consequently, the conductance change after one pulse $G_1 - G_0$ versus G_0 is positive (potentiation) for $\Delta t = +0.9$ ms and negative (depression) for $\Delta t = -1.1$ ms (see Fig. 4(c)). While $G_1 - G_0$ decreases linearly for depression, it shows a non-linear response with a maximum at 1 μS for potentiation. The initial conductance corresponds to an initial amount of QD-localized charges n_0 and thus controls the threshold voltages for charging and discharging (as shown in Fig. 1(d) for V_{d}). For decreasing n_0 (corresponds to increasing G_0), the discharging voltage is lowered and the charging voltage is raised linearly because both are proportional to $n_0 e/C$. Thus larger initial conductance values enhance the times T_{d} and T_{c} for constant bias voltages which in turn lead to larger absolute values of $G_1 - G_0$ (see equation (3)). The proportionality between V_{c} and n_0 is directly reflected in the linear $G_1 - G_0$ (G_0) - curve for a time difference of -1.1 ms. For potentiation, the linear increase is superimposed by a decline, which originates from the saturation of the conductance at the maximum value (discharged QD). In equation (3), n_- correspond to the number of electrons that tunnel out of the QD. This number is limited by n, i.e. $n_- \leq n$. For $G_0 > 1$ μS, the number of tunneling electrons equals n. Consequently, this number is reduced for increasing G_0 which according to equation (3) lowers the absolute conductance change.

Fig. 4(d) presents the relative conductance change after a single pulse versus the initial conductance. ΔG is almost constant and independent on the initial conductance value for depression, but ranges from 0 to 120 % for potentiation. Similar findings in hippocampal neurons showed relative changes of synaptic strength (absolute change divided by initial value) that depend on the initial strength for potentiation but are constant for depression, which is an important stability feature of STDP models [8, 11]. The reason therefore is that the synaptic strength triggers post-synaptic activity, and thus a constant relative change for potentiation would cause infinite synaptic strengths. A dependency of the relative change on the initial strength prevents this positive feedback and ensures converging synaptic strengths [11]. With the relative conductance change dependent on the initial conductance value, memristor-based synapses thus allow to prevent the positive feedback in artificial neural networks, where the pulses are generated intrinsically by post-synaptic activities, and ensure converging conductances.

Conductance traces versus N for 200 consecutive pulse pairs are displayed in Fig. 5(a). In the following, pulse pairs of pre- and post-synaptic pulses with negative and positive time differences are labeled as depression and potentiation pulses, respectively. The data in Fig. 5(a) was measured by applying N_{d} depression pulses with time

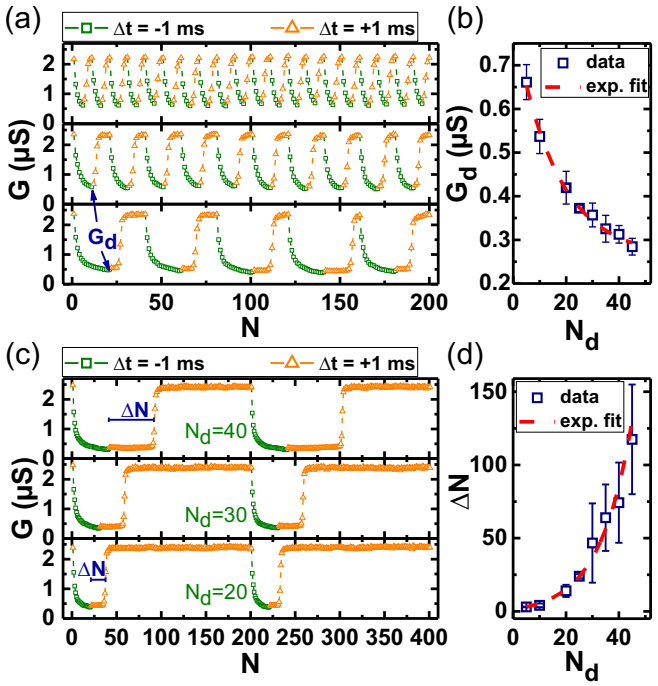

FIG. 5. **(a)** Conductance traces for 200 consecutive pulse pairs with alternating time difference. G is depressed and potentiated depending on the sign of Δt. The curves represent $N_{\mathrm{d}} = N_{\mathrm{p}} = 5$, 10 and 20 from top to bottom. **(b)** Conductance G_{d} after N_{d} depression pulses versus N_{d}. G_{d} decreases exponentially with increasing number of depression pulses. **(c)** Conductance traces for 400 consecutive pulse pairs with $N_{\mathrm{p}} = 200 - N_{\mathrm{d}}$. Applying N_{d} depression pulses requires ΔN pulses to raise G up to 50 % of the maximum value. ΔN versus N_{d} shows an exponential dependency, as displayed in **(d)**.

difference of -1 ms, followed by N_{p} potentiation pulses with time difference of $+1$ ms. The amplitude of V_{pr} was raised from 4.2 to 4.5 V to realize large positive conductance changes. The curves represent $N_{\mathrm{d}} = N_{\mathrm{p}} = 5$, 10 and 20 from top to bottom. Since the conductance can be decreased for negative and increased for positive time differences, it alternates periodically by inverting the temporal order of the pulses. The conductance value G_{d} after N_{d} depression pulses (before potentiation) shows an exponential decay versus N_{d}, as shown in Fig. 5(b). The dashed line represents the exponential fit function according to equation (3). The conductance reduction per pulse is lowered for larger N_{d} and thus many pulses are necessary to reduce G_{d} to zero. Information learned by previous potentiation is stored for a long time because of the intrinsic non-volatile memory functionality of memristors. The storage capability enables long-term storage (several days at 4.2 K for the present device) of conductance values even for zero bias, which is advantageous compared to simple RC circuits that also show exponential conductance reductions.

Conductance traces for different numbers of depression

and potentiation pulses $N_\mathrm{p} = 200 - N_\mathrm{d}$ are presented in Fig. 5(c) for 400 consecutive pulse pairs. The number of potentiation pulses ΔN to raise the conductance up to 50 % of the maximum value increases for larger N_d (lower G_d). The exponential increase of ΔN versus N_d in Fig. 5(d) can be explained bearing in mind that the application of more depression pulses leads to an enhanced amount of QD-localized charges. Thus the threshold voltage for discharging shifts towards larger values (see Fig. 1(d)) and the time interval T_d for the consecutive potentiation is lowered. According to equation (3), more pulses are needed to compensate the reduction of T_d. This explains the exponential $\Delta N - N_\mathrm{d}$ dependence as shown in Fig. 5(d). A correlation between the thresholds for potentiation and depression on the initial synaptic strength (here G_0) was also observed in the goldfish Mauthner cell [41]. Our findings of the $\Delta N - N_\mathrm{d}$-dependence enables the implementation of a memory-dependent induction of learning. Here, the number of depression pulses controls the strength before potentiation is induced by learning. The increase of ΔN for large N_d (small initial strengths) implies that potentiation and thus learning is more effective for larger initial strengths, which corresponds to the memory of previous learning processes.

VI. OPTICAL CONDUCTANCE-CONTROL

So far, the presented results may be reproducible with Si-based floating gate transistors with advantages of reduced dimensionality, room temperature operation and CMOS compatibility [24]. The presented device is based on a GaAs/AlGaAs heterostructure and it is thus fully compatible with other III-V based and state-of the art optoelectronic semiconductor devices. Due to its direct band gap, the material offers better absorption coefficients compared to similar silicon based device realizations and hence allow to control the memristance by electrical and low power optical pulses as shown in Figs. 6 and 7. For the optical excitation, a red light emitting diode (LED) with wavelength $\lambda = 632$ nm was placed beside the device. The LED illuminates the whole device as illustrated in Fig. 6(a). No (shadow) masks with tunable transmission or microscope objectives were used to focus the light, which would be essential to control single devices in a network. The reported light powers correspond to the full LED emission power and are hence an upper limit of the light power that influences the device operation. Fig. 6(b) depicts current-voltage-characteristics under cw-illumination. The LED was operated below the threshold voltage with output powers below 1 nW (detection limit of our photosensor). For a current of 10 μA, the excitation power equals 1 nW. For increasing LED currents and hence light powers, the width of the plateau with almost zero conductance around zero bias

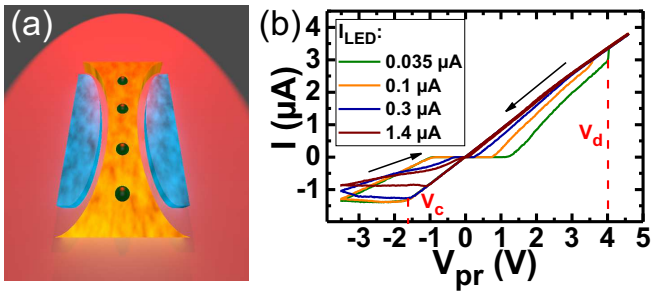

FIG. 6. **(a)** For optical excitation, the red LED was placed beside the device and illuminates the whole sample. **(b)** Current-voltage-characteristics under cw-illumination with light powers below 1 nW. The vertical red lines indicate the charging and discharging voltages for a LED current of 0.035 μA.

and therefore the amount of localized charges decreases. Thus the QD can be discharged optically. We explain the optically activated discharging by intra-band absorption, which depopulates the quantum dot when an electric field is present.[42]

Fig. 7(a) shows the conductance of the memristor versus number of excited light pulses. Instead of cw-illumination as in Fig. 6(b), the memristor was excited with pulses with widths of 10 μs and different light powers. Before the measurement ($N = 0$), the QD was charged and thus the conductance is low. For a light power of 1700 nW, the conductance starts to increase after 140 pulses and saturates at 3.5 μS after 2000 pulses. For decreasing light power, more pulses are required to raise the conductance above zero. The conductance remains unaltered for 2000 pulses with a power of 3 nW and below. Because the amount of transferred electrons is controlled by the width and the power of the light pulses, i.e. the number of incoming photons, larger excitation powers enables discharging with shorter light pulses. In Ref. [43], photo-induced charging of the QD in a similar structure was demonstrated with light in the telecommunication range. Thus we believe that the presented device allows bi-directional, light-induced conductance changes.

VII. ARITHMETIC COMPUTING

The device with its optical control of the QD localized charge and state-dependent threshold voltage for discharging is a basic component to perform arithmetic operations with optical pulses. Fig. 7(b) displays the conductance versus pulse number for optical and electrical excitation. We excited the memristor with 10 consecutive light pulses with a light power of 1 nW and a width of 10 ms (see Fig. 7(c) for time trace of the applied pulses). Each optical pulse (green) is followed by an electrical pulse (blue) with an amplitude of 4.46 V and a width of 10 ms. After each pulse pair, we deter-

mined the conductance of the memristor by applying a read-out pulse with amplitude 1.3 V. Before the measurement ($N = 0$ in Fig. 7(b)), the QD was charged by an initializing pulse with an amplitude of −3.8 V and thus the conductance is small. Applying only electrical pulses (switched off LED), the conductance remains almost unaltered up to ten pulses. Because the discharging voltage is larger than the amplitude of 4.46 V, the QD is not completely discharged and the conductance is not affected. For electrical and optical excitation, the conductance is raised successively. Each light pulse partially discharges the QD and thus enhances the conductance and reduces the discharging voltage (see Fig. 1(d)). After the 9th pulse, the discharging voltage is smaller than the electrical pulse amplitude of 4.46 V and the QD becomes fully discharged. A steep increase of the conductance occurs, as shown in Fig. 7(b). With the well pronounced conductance enhancement after the 9th pulse, the memristor is suitable for basic arithmetic operations as counting or adding in base 10. From 1 to 9 pulses, the conductance increases from 0.09 μS to 1.16 μS and for the tenth pulse a sudden raise of the conductance to 2.2 μS is observed. An addition can be performed by applying specific numbers of optical pulses that represent the addends. Multidigit operations are required if the sum of the addition exceeds the base and can be realized by combining several memristors and reset circuits to a network [44]. The reset circuits set the state variable to the initial value (reset to zero) and additionally provide the carry signal for the next significant bit. After the operation, the conductance corresponds to a certain pulse number, which is the result of the addition. In analogy to the implementations in Ref. [45], subtraction, multiplication and division can be performed. The large conductance enhancement after the tenth pulse is only possible because of the state-dependent threshold voltage for discharging and allows to trigger the reset with high accuracy and low impact of undesirable readout noise. For practical applications, this well-defined conductance state for a discharged QD triggers the release of an initialization pulse, which can be employed by additional circuitry (on-chip fabrication of comparator). In analogy to synapses in neural networks, the memristor combines processing of information and memory. The result of the arithmetic operation is stored as conductance of the memristor. Similar results have been reported for phase change materials with much larger excitation powers [45]. Here, the direct band gap leads to high absorption coefficients and the device structure with a single QD controlling the memristance allows to tune the conductance state by absorbing only a low number of photons. The optical control of the QD charge thus employs an efficient and low power possibility for arithmetic operations of light pulses.

Fig. 8(a) depicts the conductance versus number of applied light pulses with power of 1 nW and different widths of 3.1, 4.4 and 5.6 ms. The initializing pulse was

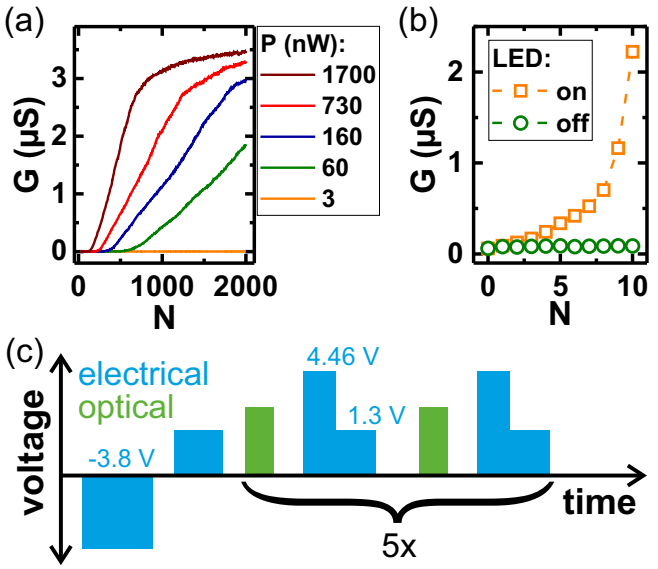

FIG. 7. **(a)** Conductance versus number of optical pulses with different light powers. **(b)** Conductance traces for 10 consecutive electrical pulses (LED: off) and pulse pairs of electrical and optical pulses (LED: on). **(c)** Schematic time trace of the applied electrical (blue) and optical (green) pulses.

lowered to −4.0 V and the electrical pulses raised to 1.5 (read-out) and 5.0 V. For a width of 3.1 ms, the conductance increases above 2.5 μS for the tenth pulse. Raising the width to 4.4 and 5.6 ms, only 8 and 6 pulses are required to discharge the QD, respectively. The color plot in Fig. 8(b) shows that the number of pulses required to discharge the QD can be tuned from one to ten and thus arithmetic operations from binary to decimal bases are possible. The large width of the light pulses (in the order of ms) was chosen to be comparable to the width of the electrical pulses. Arithmetic operations were also demonstrated in Ref. [46] with an opto-electronic resistive switching memory. However, light pulses with widths of seconds were used and a linear dependency between the current of the device and the pulse number was shown. Here, the non-linear increase of the conductance allows to clearly distinguish the states after the 9th and 10th pulse for base-10 operations. In addition, the base can be controlled by the width of the light pulses. This is especially beneficial to perform divisions in analogy to Ref. [45], where the number of pulses until a given threshold is exceeded has to be equal to the divisor. Thus our device is advantageous, because it allows to tune the number of pulses that are required to exceed the threshold solely by the width of the optical pulses.

VIII. CONCLUSION

In summary, we presented an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic

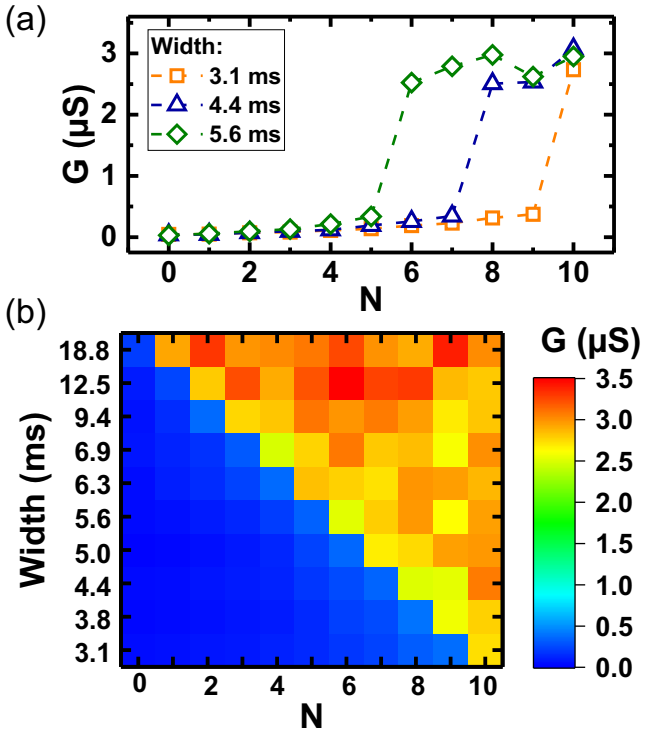

FIG. 8. **(a)** Conductance versus pulse number for widths of 3.1, 4.4 and 5.6 ms. **(b)** Color plot of the conductance versus number of electrical and optical pulse pairs. The conductance is shown for different widths of the optical pulses.

computing. Similar to synaptic strength in neural networks, the conductance is controlled by the time difference of incoming voltage pulses. In addition, the threshold voltages to switch the conductance of the device were shown to be state-dependent, which emerges from the interplay of a memristance with a memcapacitance. In contrast to other realizations of memristors, [47–49] memristance and memcapacitance switching of the presented device are observed between different terminals. The memristance is measured in the two-terminal geometry and the memcapacitance between the lateral gates and the wire. Thus the state of the device controls the charging and discharging voltages via the gate-channel-capacitance (intrinsic feedback). This may enable the implementation of memory-dependent induction of learning or the realization of counters and integrate-and-fire neurons. Here we exploited the feedback to show the capability of performing arithmetic operations in different bases with clearly distinguishable reset states.

The large pulse widths of several ms and low operation temperature prevent immediate application of the presented device in artificial neural networks. The maximum operation temperature of the device may be enhanced to room temperature by tuning the material composition of the quantum dots and the surrounding matrix [31, 50]. The widths of the pulses can be reduced by increasing the amplitude and power of the electrical and optical pulses, respectively. Write times of 6 ns have been already reported for InAs quantum dots in a GaAs matrix [51]. The presented results demonstrate the capability of emulating synaptic functionalities in combination with performing basic arithmetic operations in different bases and may trigger future research regarding the material composition to enhance the maximum operation temperature. With operation at room temperature, the device may be employed in memristor-based non-von Neumann architectures to implement brain-inspired computing with a memory-dependent induction of learning.

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[1] B. Pakkenberg, D. Pelvig, L. Marner, M. J. Bundgaard, H. J. G. Gundersen, J. R. Nyengaard, and L. Regeur, "Aging and the human neocortex," Experimental Gerontology **38**, 95 (2003).
[2] J. T. Trachtenberg, B. E. Chen, G. W. Knott, G. Feng, J. R. Sanes, E. Welker, and K. Svoboda, "Long-term in vivo imaging of experience-dependent synaptic plasticity in adult cortex," Nature **420**, 788 (2002).
[3] B. Lendvai, E. A. Stern, B. Chen, and K. Svoboda, "Experience-dependent plasticity of dendritic spines in the developing rat barrel cortex in vivo," Nature **404**, 876 (2000).
[4] T. V. P. Bliss and G. L. Collingridge, "A synaptic model of memory: long-term potentiation in the hippocampus," Nature **361**, 31 (1993).
[5] S. Song, K. D. Miller, and L. F. Abbott, "Competitive Hebbian learning through spike-timing-dependent synaptic plasticity," Nature Neuroscience **3**, 919 (2000).
[6] R. C. Froemke and Y. Dan, "Spike-timing-dependent synaptic modification induced by natural spike trains," Nature **416**, 433 (2002).
[7] L. I. Zhang, H. W. Tao, C. E. Holt, W. A. Harris, and M.-M. Poo, "A critical window for cooperation and competition among developing retinotectal synapses," Nature **395**, 37 (1998).
[8] G. Q. Bi and M. M. Poo, "Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type," The Journal of Neuroscience **18**, 10464 (1998).
[9] W. C. Abraham and W. P. Tate, "Metaplasticity: a new vista across the field of synaptic plasticity," Progress in Neurobiology **52**, 303 (1997).
[10] W. C. Abraham, "Metaplasticity: tuning synapses and networks for plasticity," Nature Reviews Neuroscience **9**, 387 (2008).
[11] M. C. van Rossum, G. Q. Bi, and G. G. Turrigiano, "Stable Hebbian learning from spike timing-dependent

plasticity," The Journal of Neuroscience **20**, 8812 (2000).
[12] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," Nano Letters **10**, 1297 (2010).
[13] B. Linares-Barranco and T. Serrano-Gotarredona, "Memristance can explain spikt-time-dependent-plasticity in neural synapses," Nature Precedings , hdl:10101/npre.2009.3010.1. (2009).
[14] D. Kuzum, R. G. D. Jeyasingh, B. Lee, and H.-S. P. Wong, "Nanoelectronic programmable synapses based on phase change materials for brain-inspired computing," Nano Letters **12**, 2179 (2012).
[15] W. He, K. Huang, N. Ning, K. Ramanathan, G. Li, Y. Jiang, J. Sze, L. Shi, R. Zhao, and J. Pei, "Enabling an integrated rate-temporal learning scheme on memristor," Scientific reports **4**, 4755 (2014).
[16] C. Zamarreño Ramos, L. A. Camuñas Mesa, J. A. Perez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, "On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex," Frontiers in Neuroscience **5**, 26 (2011).
[17] L. O. Chua, "Memristor - the missing circuit element," IEEE Trans. Circuit Theory **18**, 507 (1971).
[18] L. O. Chua and S. M. Kang, "Memristive devices and systems," Proceedings of the IEEE **64**, 209 (1976).
[19] Y. V. Pershin and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," Advances in Physics **60**, 145 (2011).
[20] M. Ziegler, M. Oberländer, D. Schroeder, W. H. Krautschneider, and H. Kohlstedt, "Memristive operation mode of floating gate transistors: a two-terminal MemFlash-cell," Applied Physics Letters **101**, 263504 (2012).
[21] P. Maier, F. Hartmann, T. Mauder, M. Emmerling, C. Schneider, M. Kamp, S. Höfling, and L. Worschech, "Memristive operation mode of a site-controlled quantum dot floating gate transistor," Applied Physics Letters **106**, 203501 (2015).
[22] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells an overview," Proceedings of the IEEE **85**, 1248 (1997).
[23] J. Brewer and M. Gill, *Nonvolatile memory technologies with emphasis on flash* (Wiley-IEEE Press, New Jersey, 2008).
[24] Y. Nishi, *Advances in non-volatile memory and storage technology* (Woodhead Publishing, Cambridge, 2014).
[25] B. Prince, *Vertical 3D memory technologies* (John Wiley & Sons, West Sussex, 2014).
[26] N. Kirstaedter, N. N. Ledentsov, M. Grundmann, D. Bimberg, V. M. Ustinov, S. S. Ruvimov, M. V. Maximov, P. S. Kop'ev, Z. I. Alferov, U. Richter, P. Werner, U. Gosele, and J. Heydenreich, "Low threshold, large T_0 injection laser emission from (InGa)As quantum dots," Electronics Letters **30**, 1416 (1994).
[27] Z. Yuan, B. E. Kardynal, R. M. Stevenson, A. J. Shields, C. J. Lobo, K. Cooper, N. S. Beattie, D. A. Ritchie, and M. Pepper, "Electrically driven single-photon source," Science **295**, 102 (2002).
[28] C. L. Salter, R. M. Stevenson, I. Farrer, C. A. Nicoll, D. A. Ritchie, and A. J. Shields, "An entangled-light-emitting diode," Nature **465**, 594 (2010).
[29] M. Kroutvar, Y. Ducommun, D. Heiss, M. Bichler, D. Schuh, G. Abstreiter, and J. J. Finley, "Optically programmable electron spin memory using semiconductor quantum dots," Nature **432**, 81 (2004).
[30] S. Cortez, O. Krebs, S. Laurent, M. Senes, X. Marie, P. Voisin, R. Ferreira, G. Bastard, J.-M. Gérard, and T. Amand, "Optically driven spin memory in n-doped InAs-GaAs quantum dots," Physical Review Letters **89**, 207401 (2002).
[31] A. Marent, T. Nowozin, M. Geller, and D. Bimberg, "The QD-Flash: a quantum dot-based memory device," Semicond. Sci. Technol. **26**, 014026 (2011).
[32] C. Schneider, A. Huggenberger, T. Sünner, T. Heindel, M. Strauß, S. Göpfert, P. Weinmann, S. Reitzenstein, L. Worschech, M. Kamp, S. Höfling, and A. Forchel, "Single site-controlled In(Ga)As/GaAs quantum dots: growth, properties and device integration," Nanotechnology **20**, 434012 (2009).
[33] I. M. Filanovsky and S. T. Lim, "Temperature sensor applications of diode-connected MOS transistors," IEEE ISCAS **2**, 149 (2002).
[34] L. O. Chua, "If its pinched its a memristor," Semicond. Sci. Technol. **29**, 104001 (2014).
[35] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature **453**, 80 (2008).
[36] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: memristors, memcapacitors, and meminductors," Proceedings of the IEEE **97**, 1717 (2009).
[37] A. L. Hodgkin and A. F. Huxley, "Action potentials recorded from inside a nerve fibre," Nature **144**, 710 (1939).
[38] P. Maier, F. Hartmann, M. Emmerling, C. Schneider, S. Höfling, M. Kamp, and L. Worschech, "Charging dynamics of a floating gate transistor with site-controlled quantum dots," Applied Physics Letters **105**, 053502 (2014).
[39] L. Guo, E. Leobandung, and S. Y. Chou, "A silicon single-electron transistor memory operating at room temperature," Science **275**, 649 (1997).
[40] B. Marquardt, A. Beckel, A. Lorke, A. D. Wieck, D. Reuter, and M. Geller, "The influence of charged InAs quantum dots on the conductance of a two-dimensional electron gas: mobility vs. carrier concentration," Applied Physics Letters **99**, 223510 (2011).
[41] X.-D. Yang and D. S. Faber, "Initial synaptic efficacy influences induction and expression of long-term changes in transmission," Proc. Natl. Acad. Sci. USA **88**, 4299 (1991).
[42] T. Nozawa, H. Takagi, K. Watanabe, and Y. Arakawa, "Direct observation of two-step photon absorption in an InAs/GaAs single quantum dot for the operation of intermediate-band solar cells," Nano Letters **15**, 4483 (2015).
[43] S. Göpfert, L. Worschech, S. Lingemann, C. Schneider, D. Press, S. Höfling, and A. Forchel, "Room temperature single-electron memory and light sensor with three-dimensionally positioned inas quantum dots," Applied Physics Letters **97**, 222112 (2010).
[44] Y. V. Pershin, L. K. Castelano, F. Hartmann, V. Lopez-Richard, and M. Di Ventra, "A memristive pascaline," Cir. & Syst. II, IEEE Trans. (2016), 10.1109/TCSII.2016.25303

[45] C. D. Wright, Y. Liu, K. I. Kohary, M. M. Aziz, and R. J. Hicken, "Arithmetic and biologically-inspired computing using phase-change materials," Advanced Materials **23**, 3408 (2011).

[46] H. Tan, G. Liu, X. Zhu, H. Yang, B. Chen, X. Chen, J. Shang, W. D. Lu, Y. Wu, and R.-W. Li, "An optoelectronic resistive switching memory with integrated demodulating and arithmetic functions," Advanced Materials **27**, 2797 (2015).

[47] L. Qingjiang, A. Khiat, I. Salaoru, C. Papavassiliou, X. Hui, and T. Prodromakis, "Memory impedance in TiO_2 based metal-insulator-metal devices," Scientific Reports **4**, 4522 (2014).

[48] A. A. Bessonov, M. N. Kirikova, D. I. Petukhov, M. Allen, T. Ryhänen, and M. J. A. Bailey, "Layered memristive and memcapacitive switches for printable electronics," Nature Materials **14**, 199 (2015).

[49] Z. B. Yan and J.-M. Liu, "Coexistence of high performance resistance and capacitance memory based on multilayered metal-oxide structures," Scientific Reports **3**, 2482 (2013).

[50] T. Nowozin, D. Bimberg, K. Daqrouq, M. N. Ajour, and M. Awedh, "Materials for future quantum dot-based memories," Journal of Nanomaterials **2013**, 1 (2013).

[51] M. Geller, A. Marent, T. Nowozin, D. Bimberg, N. Akçay, and N. Öncan, "A write time of 6 ns for quantum dot-based memory structures," Applied Physics Letters **92**, 092108 (2008).