Logical Stochastic Resonance with a Coulomb-Coupled Quantum-Dot Rectifier

P. Pfeffer,[1] F. Hartmann,[1] S. Höfling,[1,2] M. Kamp,[1] and L. Worschech[1]

[1]*Technische Physik, Physikalisches Institut, Universität Würzburg and Wilhelm Conrad Röntgen Research Center for Complex Material Systems, Am Hubland, D-97074 Würzburg, Germany*

[2]*SUPA, School of Physics and Astronomy, University of St Andrews, St Andrews KY16 9SS, United Kingdom*

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Noise is mostly considered to be an adverse factor in electronics. Yet, effects like logical stochastic resonance (LSR) can render electronic fluctuations useful. Here, we study LSR in a system consisting of two Coulomb-coupled quantum dots (QDs). We observe that voltage fluctuations applied to one of the QDs lead to a rectified and controllable current in the other QD. The interplay between applied noise and gate voltages enables our system to offer logic AND, OR, NAND, and NOR gate functionalities, which can be switched by either a variation of the noise or of a single gate voltage. For an optimal amount of noise, all four functionalities can be toggled by changing solely one single gate voltage. The presented results may prove beneficial for future autonomous, noise-tolerant, and energy-efficient electronics.

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I. INTRODUCTION

In recent years, the exploitation of excess heat and noise has become a topical and significant branch of research, especially in electronics [1,2]. Reasons are, on the one hand, the decreasing signal-to-noise ratio as computational devices continue to shrink and as waste heat becomes ever harder to handle [3–5]. On the other hand, there is a trend towards sustainable, energy-efficient, and autonomous systems which profit from the recovery of excess heat and noise [6,7]. Nonlinear systems offer possibilities to make use of this noise: it can be utilized to enhance weak input signals, as is the case for effects which are based on stochastic resonance (SR) [8]. SR, phenomenologically introduced to explain the periodic occurrence of Earth's ice ages, is the beneficial interplay between a nonlinear system, a weak dynamic signal, and noise, which leads to a maximum of the signal-to-noise ratio for a nonvanishing noise floor [9]. Although introduced on a macroscopic length scale, SR has been observed in many microscopic systems ranging from biological to solid-state systems [9–11]. Besides, noise can be employed to change the functionality of nanoelectronic devices. For example, it can be used to switch a memristor to its desired resistive state [12]. Furthermore, noise is essential for logical stochastic resonance (LSR), a phenomenon where the application of noise to a system with several (logical) inputs improves the operation of a logic gate. For LSR, it occurs that the logic gate is fault tolerant and reliable in an optimal window of noise [13–15]. Moreover, a morphing between different logic gates can be achieved by a variation of the systems asymmetry or the noise floor. The switching of the individual function of elements in a larger network allows applications where a network can be programmed in a way in which it can adapt efficiently to the upcoming calculation. Reconfigurable computing represents a software- rather than a hardware-determined approach to computation which has the potential to improve computational speed and efficiency [16–18].

In many LSR systems, noise enhances the signal quality but is not sufficient for the system to produce an output by itself. It is, however, the main source for the generation of an output in cases where noise can be rectified in order to harvest energy [2,19–22]. Work in this field has led to diverse concepts including Brownian motors [23], Büttiker-Landauer motors [24,25], or piezoelectric nanogenerators [26], all of which have certain forms of symmetry breaking in common. A striking proposal of rectifying effects in electronics was recently made by Sánchez *et al.* [20] and Sothmann *et al.* [21], who investigated rectification of fluctuations in a Coulomb-coupled quantum-dot and open-cavity system, respectively. Sanchez *et al.* showed that Coulomb-coupled quantum dots can act as a rectifier which transfers each energy quantum that passes from one to the other quantum dots (QDs) to the motion of single electrons [20]. Later, Sothmann *et al.* investigated a similar design based on open QD systems (with conductances higher than the conductance quantum) exhibiting higher output currents [21].

In this paper, we present a Coulomb-coupled quantum-dot device, combining noise rectification and LSR approaches: the device generates an output current by rectification of fluctuations and exploits the interplay between the nonlinearity of the system and noise, in order to realize several Boolean logic gates when two gate electrodes are taken as logic inputs. By variation of the noise amplitude and the electrostatic potential at one of the QDs, logic AND, OR, NAND, and NOR functionalities can be obtained. We further demonstrate that a switching between

different logic gates can be realized by either a variation of the noise floor at a fixed system asymmetry or by a variation of this asymmetry while keeping the noise in an optimal range.

II. EXPERIMENT AND DISCUSSION

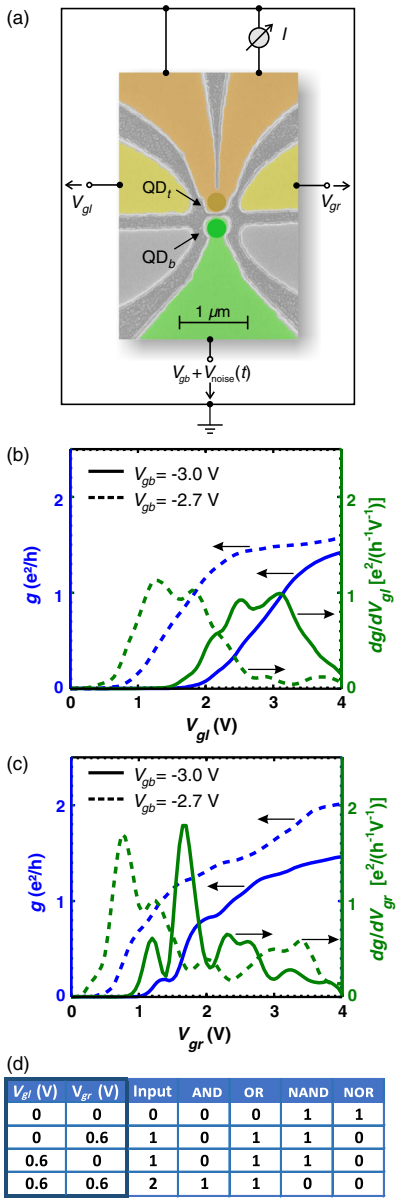
Figure 1(a) shows an electron microscopy image of the device. The sample is based on a modulation-doped GaAs/(Al, Ga)As heterostructure in which a high-mobility two-dimensional electron gas is situated about 80 nm below the surface. The heterostructure is grown via molecular beam epitaxy and the structural design is realized using electron beam lithography and dry chemical etching. It consists of two quantum dots (QD_b and QD_t) which are coupled via Coulomb interaction, one of them being connected to two electronic leads (via two quantum-point contacts, QPC_l and QPC_r), the other being connected to an electronic reservoir. The upper part of the structure can be influenced by means of two side gates where the voltages V_{gl} and V_{gr} can be applied, and by the bottom gate (the bottom reservoir) with the static voltage V_{gb} and the additional noise voltage $V_{\mathrm{noise}}(t)$. Only the upper two of the four side gates in Fig. 1(a) are used in this study (highlighted in yellow), the lower ones are left on a floating potential.

Applying noise to the lower subsystem leads to a rectified current through the upper subsystem, which is measured with a picoamperemeter. This mechanism is explained in more detail in Refs. [20–22]. In short, Coulomb coupling between the two quantum dots, in conjunction with the applied noise and conductance asymmetries between the two QPCs, lead to a rectified output current $I \propto \Lambda\sigma^2$. Here, σ is the root-mean-square value of $V_{\mathrm{noise}}(t)$ (the output of a Gaussian-distributed and spectrally flat noise source with a cutoff frequency $f =$ 20 MHz) and Λ is an asymmetry parameter which depends on the energy-dependent and the energy-independent parts of the quantum-point-contact transmissions [21],

$$\Lambda = \frac{G_l' G_r - G_r' G_l}{(G_l + G_r)^2}, \tag{1}$$

with G_i and G_i' being the energy-independent and energy-dependent part of QPC_i's conductance ($i = l, r$), respectively.

As the conductances of the QPCs, and therefore Λ, can be varied by utilizing the side gates, the system's output current I can be controlled by means of V_{gl} and V_{gr}. V_{gb} serves as an additional control parameter. This can be seen in Figs. 1(b) and 1(c), where the side-gate voltages open and close the respective channels [left channel in 1(b) and right channel in 1(c)]. There, the upper subsystem's overall conductance g is shown (blue) together with the derivatives of g (green) with respect to the respective side-gate voltage, V_{gl} or V_{gr}. The curves are shown for two different gate voltages $V_{gb} = -3.0$ V (solid lines) and -2.7 V (dotted lines). All experiments reported here are performed at 4.2 K in the dark by immersing the sample in liquid helium. As a first-order approximation, the voltage influencing a channel



(d)

V_{gl} (V)	V_{gr} (V)	Input	AND	OR	NAND	NOR
0	0	0	0	0	1	1
0	0.6	1	0	1	1	0
0.6	0	1	0	1	1	0
0.6	0.6	2	1	1	0	0

FIG. 1. (a) Electron microscopy image of the sample. The upper part of the system (orange) carries the current and electronic fluctuations are applied at the lower part (green). The logic input voltages V_{gl} and V_{gr} are applied at the upper side gates (yellow). The lower side gates are not used in the presented measurements. (b),(c) Conductances g and derivatives of the conductance dg/dV_{gl}, and dg/dV_{gr}, respectively. Opening of the left (b) and right (c) channel for $V_{gb} = -3.0$ V (solid lines) and $V_{gb} = -2.7$ V (dotted lines). In (b), $V_{gr} = 0$ V; in (c), $V_{gl} = 0$ V. (d) Input definition and logic truth table. The logical Input values are defined by the combinations of the side-gate voltages V_{gl} and V_{gr}, which take either the high-level 0.6 V or the low-level 0 V. Furthermore, the outputs (1 or 0, corresponding to high or low) are shown for the relevant logic gates.

is the superposition of its side-gate voltage and V_{gb}. Thus, higher V_{gb} shifts the curves to lower V_{gl} and V_{gr} values. As the side-gate voltages are increased, the respective channels' conductance increases. Conductance traces have an initial steep increase and subsequent flattening in common. In the derivatives, this expresses itself in an initial peak and a subsequent lowering. The conductance derivatives represent a magnitude proportional to the energy-dependent part of the conductance. The side-gate voltages are thus capable of manipulating the asymmetry parameter Λ and hence the resulting output current.

Considering V_{gl} and V_{gr} as inputs and I as output, several logic gates can be realized. To facilitate later illustration, we summarize side-gate voltage combinations to the single parameter Input, which is defined in Fig. 1(d). Figure 2 shows the rectified output current in several color plots, depending on V_{gl} and V_{gr} for various σ and V_{gb}. We define the output to be high if $I \geq 15$ nA and to be low if $I < 15$ nA. Accordingly, the numbers corresponding to the white rectangles' corners (0 for low and 1 for high) in Fig. 2 show the output level for each plot and each input configuration. The numerical value for the output threshold is chosen to be at approximately half the maximally measured current, while low and high inputs are correspondingly chosen in order to be used with the measured data. Still, all of them could, in a certain range, also be set differently (see also discussion of Fig. 3 below).

Several input configurations lead to Boolean logic-gate functionalities. Those are pointed out by the name of the functionality inside the corresponding plots. Particularly for $\sigma = 67.5$ mV, a sole change of V_{gb} can switch the device functionality from a nonlogic functionality to a NOR, a NAND, an OR, an AND, and back to a nonlogic functionality (second row in Fig. 2, yellow background). This offers the possibility to design complex logical architectures by using a multitude of the same devices and to alter the overall functionality of the architecture by changing the individual functionality of one or more of the devices involved, employing controllable gate voltages. Whereas for $V_{gb} = -2.75$ V, a sole variation of σ is able to switch

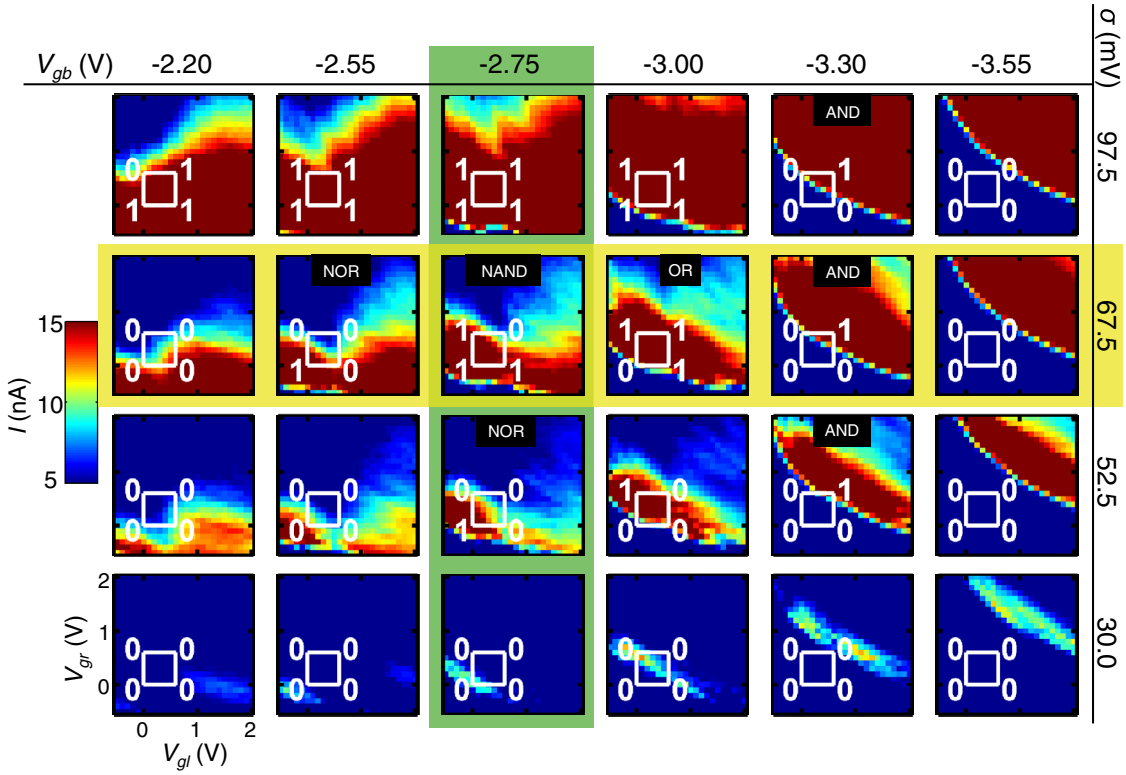


FIG. 2. Color plots of the output current versus V_{gl} and V_{gr} for several different σ and V_{gb}. The corners of the white rectangles show the position of different side-gate input-voltage configurations, where V_{gl} and V_{gr} take either the high or the low level. The output current levels are defined to be high (1) if $I \geq 15$ nA and to be low (0) if $I < 15$ nA. To ensure a better visibility of the regions where $I \geq 15$ nA, the color range ends at 15 nA. Measured currents can reach higher values, though (see Figs. 3 and 4). The numbers next to the white rectangles' corners mark the logical output. Depending on V_{gb} and σ, the device shows different logic functionalities (cf. text in the respective color plots). For $V_{gb} = -2.75$ V (third column, highlighted in green), the variation of σ allows a switching between no logic functionality, NOR, and NAND functionalities. Correspondingly, for $\sigma = 67.5$ mV (second row, highlighted in yellow), the variation of V_{gb} allows a switching between no logic functionality, NOR, NAND, OR, and AND functionalities.

between NAND, NOR, and nonlogic functionalities (third column in Fig. 2, green background). The logic-gate switching caused by a sole variation of the noise floor can be employed in networks in which the output is invariant to a commutation of logic elements. For instance, a full adder's output does not change under a NOR or NAND commutation [27]. Here, the noise-dependent switching of the logic functionality due to effects like local heating from hot spots can be of interest for practical applications. Altogether, transitions between different logic functionalities can be obtained by changing either the noise standard deviation, as for instance shown for a different logical stochastic resonance system in Ref. [28], or by changing the control parameter V_{gb}, as discussed in Refs. [13,14]. No logical functionality can be observed for $\sigma = 0$, as well as for $\Lambda \approx 0$ (which is, for instance, the case for large negative V_{gb}), which results in $I \approx 0$.

To explain the experimental findings, we model the system's output current using the following equations [21,29,30]:

$$I = c\Lambda G_{\text{eff}}\sigma^2, \tag{2}$$

$$G_i = \frac{e^2/h}{1+\exp\left(-\frac{e(\eta_{i,i}V_i + \eta_{i,j}V_i + \eta' V_{gb}) + E_{0,i}}{k_B T}\right)}, \tag{3}$$

$$G_i{}' = \frac{dG_i}{dV_i}. \tag{4}$$

In Eq. (2), c is a scaling factor, Λ is the asymmetry parameter [cf. Eq. (1)], and $G_{\text{eff}} = G_l + G_r$ is the effective conductance of the upper subsystem [21]. In Eq. (3), $i = l$ or $i = r$, e is the elementary charge, k_B is the Boltzmann constant, and T the environmental temperature (4.2 K). $\eta_{i,i}$ is the gate efficiency of gate i ($i = l, r$) with respect to QPC$_i$, $\eta_{i,j}$ is the efficiency of gate i with respect to QPC$_j$ (with $i \neq j$), and η' is the efficiency of the bottom gate with respect to the entire upper channel. $E_{0,i}$ accounts for the energetic offset of QPC$_i$ resulting from the lateral confinement potential.

As σ controls the magnitude of the output current, it influences the size of the (red) high-current regions in Fig. 2, whereas V_{gb} shifts this region on the diagonal axis from small to high V_{gl} and V_{gr} [as a first approximation; cf. Figs. 1(b) and 1(c)].

Figures 3(a) and 3(b) present simulations of I for the three logic-input configurations (Input = 0, 1, and 2) against σ and V_{gb}, respectively. The parameters $c, \eta_{i,i}, \eta_{i,j}, \eta'$, and $E_{0,i}$ are fitted to obtain outputs comparable to the measured data. This leads to the following values: $c = 0.024$, $\eta_{l,l} = 7.5 \times 10^{-4}$, $\eta_{l,r} = 6.5 \times 10^{-4}$, $\eta_{r,r} = 4.0 \times 10^{-4}$, $\eta_{r,l} = 4.0 \times 10^{-4}$, $\eta' = 19 \times 10^{-4}$,

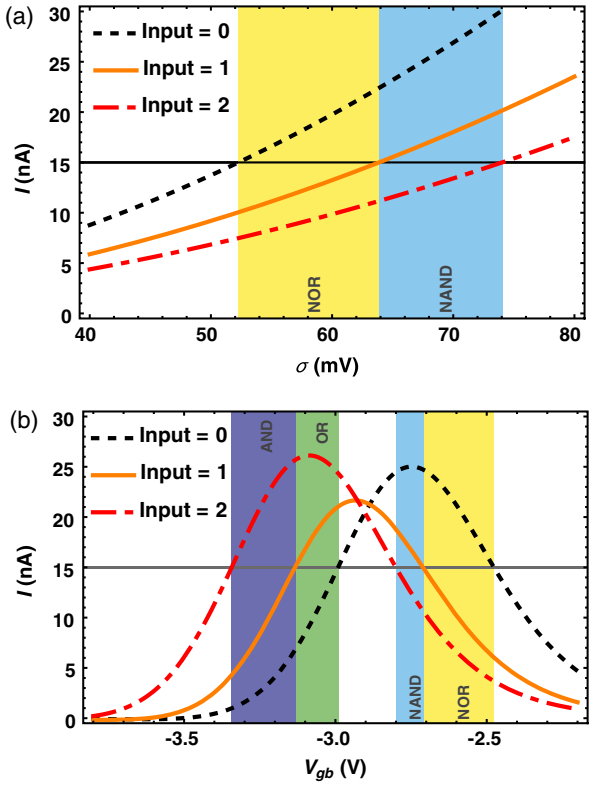


FIG. 3. Simulation of the output current depending on σ [in (a), $V_{gb} = -2.75$ V] and V_{gb} [in (b), $\sigma = 67.5$ mV] for Input = 0, 1, and 2. The black lines designate the threshold between low and high. Regions where logical functionalities occur are particularly highlighted. The simulations in (a) and (b) correspond to the experiments shown in the third column and the second row in Fig. 2, respectively.

$E_{0,l} = 6.0 \times 10^{-3}$ eV, and $E_{0,r} = 5.2 \times 10^{-3}$ eV. Figure 3(a) shows the calculated curves for a constant $V_{gb} = -2.75$ V and varying σ, which correspond to the experiments presented in the second row in Fig. 2. As I increases parabolically with different slopes for the individual input configurations as σ is increased, the system starts with $I = 0$ for $\sigma = 0$ and is initially situated in a nonfunctional logic state. It then takes a NOR functionality when the Input = 0 curve crosses the threshold, and subsequently takes a NAND functionality as soon as I is above the threshold for the mixed input states (Input = 1). The system then reaches a nonfunctional logic configuration again as the current is above the threshold for all input configurations. This characteristic is independent of the numeric threshold value.

The simulation where σ is set to constant 67.5 mV while V_{gb} is varied can be seen in Fig. 3(b) and represents the experimental data shown in the third column of Fig. 2. There, going from lower to higher V_{gb}, the individual current traces successively cross the threshold from below, reach a maximum, and fall beneath the threshold again. As these crossings occur at separate V_{gb} for the different input

configurations, the system offers AND, OR, NAND, and NOR functionalities for different V_{gb}. The qualitative succession of the functionalities during a V_{gb} sweep from low to high values is the same for all thresholds larger than 0 and smaller than the lowest I value at which the individual current traces cross [approximately 20 nA in Fig. 3(b)]. For low V_{gb}, I reaches 0 because the gate voltage closes the conductive channels, whereas, for high V_{gb}, I approaches 0 since higher G_i gradually minimize Λ. In between, the current reaches a maximum. The maximal current values for Input $= 0$ and Input $= 2$ are of similar magnitude since those two input configurations are both characterized by $V_{gl} = V_{gr}$ and a variation of V_{gb} approximately shifts the region of maximal current along the $V_{gl} = V_{gr}$ axis. The maximum for Input $= 1$ is distinctly lower, because for Input $= 1$ $V_{gl} \neq V_{gr}$.

To test the time response of the particular logical stochastic gates, we apply rectangular voltages with an amplitude of 0.6 V and frequencies of 1, respectively, 0.1 Hz to V_{gl} and V_{gr}, respectively. Figures 4 and 5 show the system's output current during such switchings of the logical input. For the four different V_{gb} used for the experiments in the second row of Fig. 2, Input and the resulting output current I are shown as a function of time t in Fig. 4. The black line is drawn into the graphs to accentuate the current threshold between low and high. The variation of V_{gb} here allows us to switch between four different logic-gate functionalities. Figure 5 shows the corresponding plots for a fixed $V_{gb} = -2.75$ V and two different σ (third column in Fig. 2). In this case, the variation of σ can change the system from a NOR to a NAND gate. Having two different I values for Input $= 1$ in each graph of Figs. 4 and 5 is due to the two possible side-gate

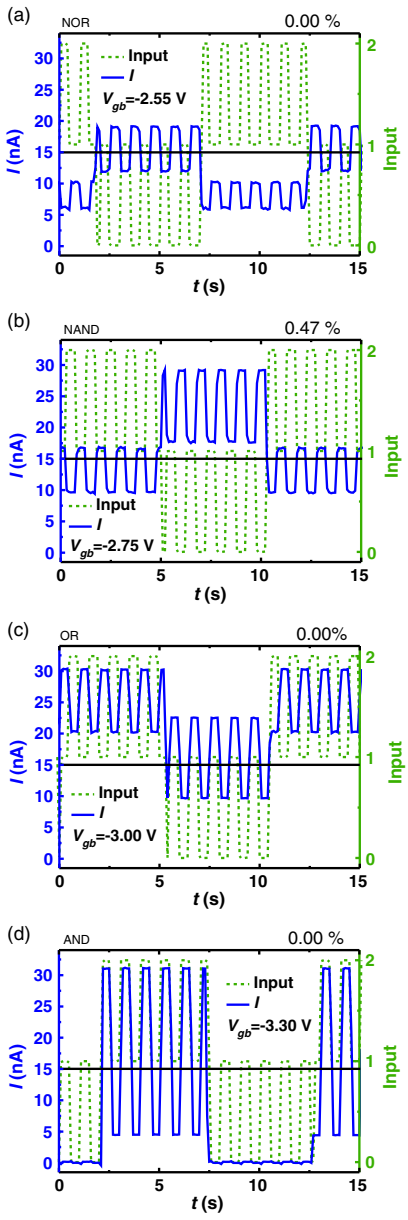


FIG. 4. Output currents I and logical input as a function of time t for $\sigma = 67.5$ mV and $V_{gb} = -2.55$ V (a), $V_{gb} = -2.75$ V (b), $V_{gb} = -3.00$ V (c), and $V_{gb} = -3.30$ V (d). The measurements correspond to the second row in Fig. 2. Panel (a) represents a NOR gate, (b) a NAND gate, (c) an OR gate, and (d) an AND gate. The black line at $I = 15$ nA designates the threshold between low and high. The measured error probabilities are displayed on top of the respective graphs.

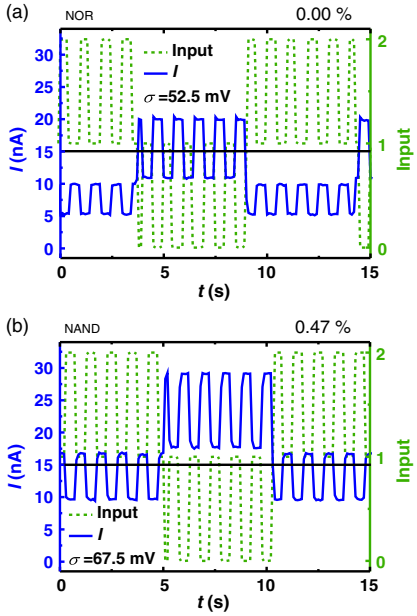


FIG. 5. Output currents I and logical input as a function of time t for $V_{gb} = -2.75$ V and $\sigma = 52.5$ mV in (a) as well as $\sigma = 67.5$ mV in (b). The measurements correspond to the third column in Fig. 2. (a) represents a NOR gate (b) a NAND gate. The black line at $I = 15$ nA designates the threshold between low and high. The measured error probabilities are displayed on top of the respective graphs.

voltage combinations in conjunction with unequal side-gate efficiencies.

In order to determine the probability of faulty switching between the output states, we measure about 4200 switches between the different logic inputs for all achievable gates and count the number of incorrect outputs. The resulting error probabilities are displayed on top of the respective graphs in Figs. 4 and 5. For the two AND gates shown in Fig. 2, but not in Figs. 4 and 5, we determine the following error probabilities: 0.00% for $\sigma_{\text{noise}} = 97.5$ mV and 1.90% for $\sigma_{\text{noise}} = 52.5$ mV. Errors are thus most probable to occur when the difference between the threshold and the output current is very small as is the case for the NAND gate and the low-noise AND gate.

III. CONCLUSION

In conclusion, we demonstrate logical stochastic resonance in a Coulomb-coupled quantum-dot device. The system can be tuned to manifest AND, OR, NAND, and NOR gate functionalities by means of the control parameters σ and V_{gb}. Remarkably, the sole variation of either of those parameters suffices to switch the system between different logic functionalities which we show in a broad range of σ and V_{gb}. Moreover, we present time-dependent logic switching for the individual logic gates as well as simulated data, supporting and complementing the experimental findings. The presented work offers potential implementation of efficient computation schemes benefiting from voltage-controlled programmable logic-gate devices which facilitate adaptation to upcoming calculations. Furthermore, it is a step towards energy saving and autonomous computing applications, allowing the use and recovery of electrical noise.

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