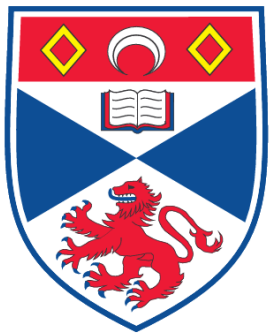
AN EMBEDDED CONTROL AND DISPLAY SYSTEM FOR A LASER-BASED MID-INFRARED HYPERSPECTRAL IMAGER

Mark Ross

A Thesis Submitted for the Degree of MPhil
at the
University of St. Andrews



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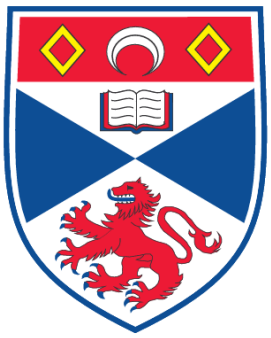

University
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St Andrews

Mark Ross

A thesis submitted to the University of St Andrews
in application for the degree of Master of Philosophy

18th July, 2008

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Abstract

Back-scatter absorption gas imaging (BAGI) is a powerful laser-based detection technique whereby the strong spectroscopic absorption features in the gaseous species of interest are exploited in order to provide an image of the otherwise invisible (to the naked eye) gas. Such a device had been under development at the University of St. Andrews for the past three years. This thesis is concerned with the work carried out in the design, construction and testing of an electronic supervisory system for such a device to both control the electro-mechanical image acquisition hardware and display the image data upon an LCD module via an on-board video driver. Two different LCD display technologies, super twisted nematic (STN) and thin film transistor (TFT), have been demonstrated and their suitability for use in this system is assessed. It was found that the refresh rate and contrast ratio of the TFT display was greatly superior to that of the STN. Frame rates in excess of 10 fps have been demonstrated with this module. In addition to the scanner, a laser management system (LMS) was designed, constructed and tested to control the laser illumination system, which is based on an intracavity optical parametric oscillator (ICOPO). This involved the development of a dual-channel PID temperature controller to stabilise various optical components located within the ICOPO illumination source, a digitally-controlled constant current source to drive the pump diode laser and a digitally controlled system for an associated Q-switch driver module. The LMS was developed as part of the miniaturisation process and resulted in one dedicated instrument replacing six individual devices required in the laboratory demonstrator. The BAGI device has now been commercialised with elements of this research program being part of the overall instrument.

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I dedicate this thesis to my loved ones - my wife Carolyn, my mother Margaret, my brother Mike, my late father Alec and indeed our beautiful daughter Abbie who was born on 22nd August 2008.

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Chapter One - Introduction

1.1 Back-Scatter Absorption Gas Imager (BAGI)

Research at the University of St Andrews has led to the development of a Backscatter Absorption Gas Imaging (BAGI) system [1,2,9] based on a novel laser source, and this system is currently being constructed for field testing as a man portable instrument. Crucial to this is the development of a dedicated electronic system capable of controlling the electro-mechanical hardware. This hardware was previously developed in readiness for demonstration and commercialisation in the near future, within the context of a portable standalone instrument. The present project is concerned with meeting these objectives through the design and realisation of electronic hardware and embedded software upon which it will depend. The micro-controlled data acquisition & visual display system and the supervisory laser management hardware are described in this report.

1.2 Advantages of a BAGI system

Gas detection is very important for many reasons from environmental and economic issues to life threatening situations and so the quicker an unwanted leak can be isolated and serviced, the chances of a serious incident involving such a leak are minimised. Current gas detection techniques are based around technologies such as gas chromatography or electronic 'point and sniff' detectors. Such techniques have adequate sensitivity and (in the case of electronic gas detectors) portability and so are ideal in a number of small-scale, low cost (for instance, domestic) applications. However, as they simply measure point concentration of the gaseous species under investigation, very little feedback is given to the operator as to the source of the leak. This can prove extremely problematic when gas leaks are detected in very large scale industrial installations. A visual picture, relayed to the operator in real time, which indicated both the presence *and position* of the detected gas would be highly desirable, and it is this feature which is exploited in the BAGI technique. Gas imaging obtains instant results helping to source the location of the leak as well as an indication of its severity.

1.3 Methane Detection with a BAGI system

The gas investigated for detection in this research project is methane (CH_4) because it is a widely used source of cheap energy found in both domestic and industrial environments. The main disadvantages of methane are that it is highly explosive when mixed with air, is a potent greenhouse gas and thus damaging to the environment and is a colourless, odourless (in its native form) molecule which is completely invisible to the human eye. The BAGI method of detection depends upon the gaseous species of interest exhibiting strong optical absorption at some illumination wavelength. In the case of methane, the highest absorption coefficients are located in the mid-infrared region at ~3.31μm, as shown in figure 1.1. The idea underpinning the BAGI technique is that if a powerful light source, of sufficient spectral purity and with a wavelength coincident with these absorption features is used to illuminate an area, any methane present within its illuminated area would very strongly absorb this light. Light not absorbed by the gas (i.e. where no gas is present) would be back-scattered (for example, from walls or pipes) and this could be collected and imaged, thus allowing the visualisation of methane. This technique is shown in figure 1.2.

Label y axis logα(A.U)

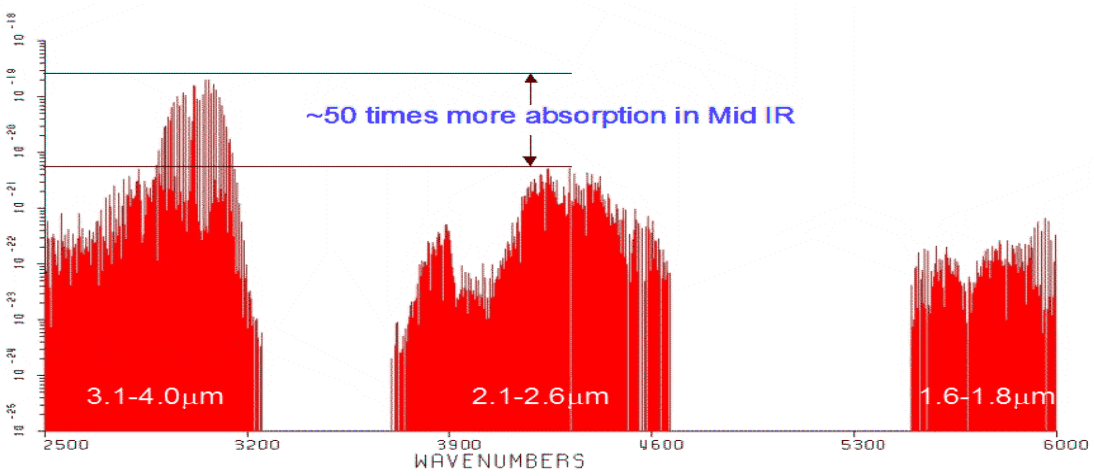

Figure 1.1: Methane absorption wavelengths [3]

1.4 BAGI Components

Gas detection with the BAGI technique requires two key sub systems; a powerful mid-infrared laser source (ideally tunable) for scene illumination and an imaging system with which to visualise the back-scattered light.

Current conventional laser systems operating in the mid-infrared band are typically characterised by low power output, very poor tunability, excessive system complexity and cost, or a combination of these. For instance, whilst lead-salt (PbS) laser diodes are relatively low cost and offer moderate temperature tunability, they emit very low (<1 mW) power and need to be cryogenically cooled in order to operate. The mid-infrared Helium-Neon laser offers more power (up to ~10 mW) but is inefficient, bulky, fragile and cannot be tuned into different absorption transitions. Clearly, a laser system exhibiting tunable, narrow linewidth and high output power characteristics from a compact, all solid-state geometry would be highly desirable in the context of this application.

1.4.1 Optical Parametric Oscillators

The technique used to achieve the power and wavelength agility required for this application in the mid-infrared spectral band is a pulsed Optical Parametric Oscillator (OPO). This development of this optical source was largely carried out before the onset of this research project and a detailed description of the physics processes underpinning its operation is somewhat outside the scope of this report. However, the basic principles of operation are briefly outlined here. The parametric process is a non-linear optical effect which operates by taking a high energy (short wavelength) photon and “splitting” it into two lower energy, and therefore longer wavelength, photons as depicted in figure 1.3. These generated photons are called the signal and idler photons, with the idler the longer wavelength of the two. By changing the properties of the non-linear crystal (for instance, it’s temperature) the wavelengths of the signal and idler can be changed, and hence any system utilising an OPO is tunable even if the laser upon which it is based is not. In this system, the wavelength of the idler wave is tuned into the methane absorption features of interest.

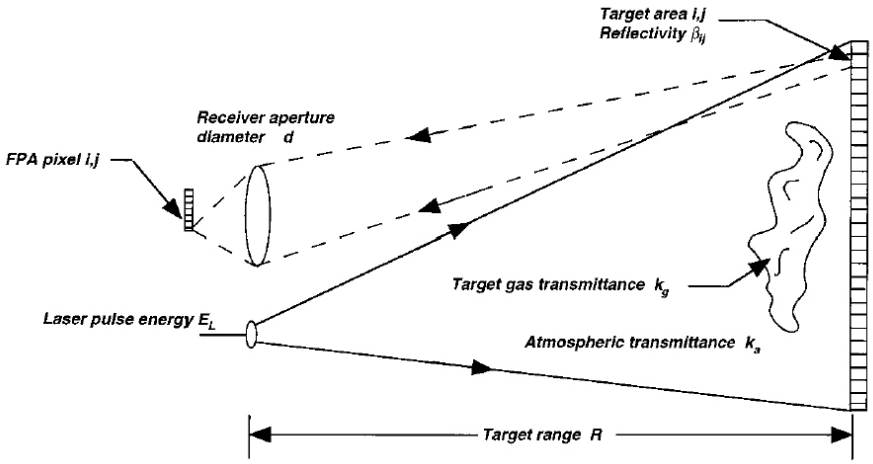

Figure 1.2 (a): An example of a BAGI system [1]

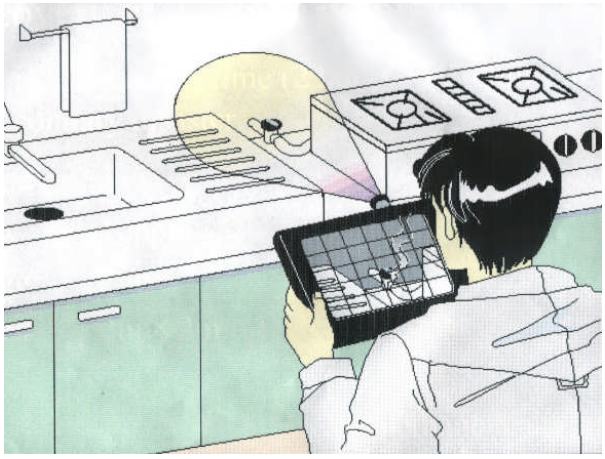

Figure 1.2 (b): Implementation of the BAGI technique

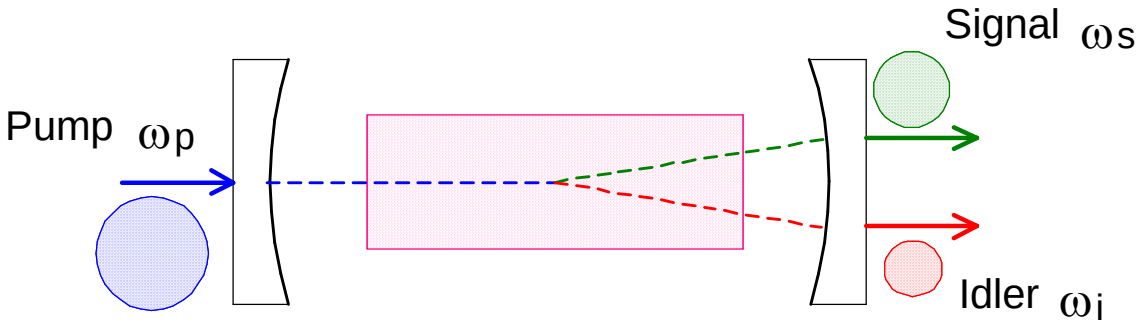

Figure 1.3 : The parametric process.

Traditionally, these devices have required somewhat excessively high input powers to reach threshold or have suffered serious stability issues. The solution to this is to place the OPO within the optical cavity of the pump laser and hence take advantage of the very high pump field found there, shown in figure 1.4.

Whilst the *intracavity OPO* (ICOPO) can be made to operate in a continuous-wave mode [4,5] the system utilised in this project was pulsed by the inclusion of an acousto-optic Q-switching element within the pump cavity to stabilise the transient dynamics of the laser. The system is capable of producing ~150 mW of broadly-tunable peak idler power at a repetition rate of >350 kHz. As we shall see later on in this report, careful triggering of the Q-switching element is required in order to synchronise the production of optical pulses with spatial pixel points.

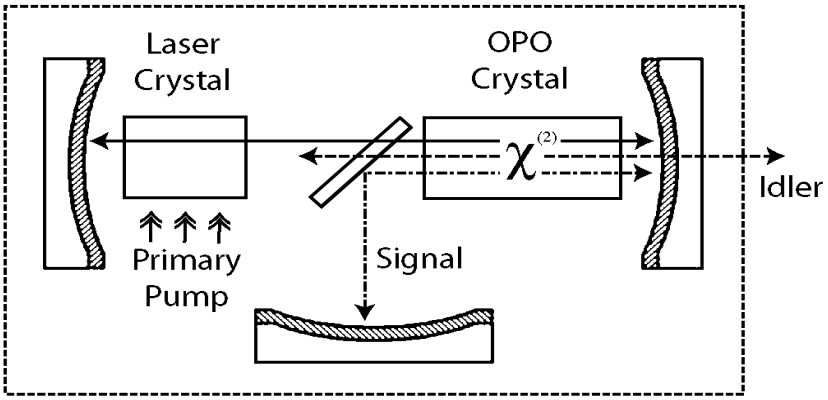

Figure 1.4 : OPO inside a laser cavity, the Intracavity OPO (ICOPO).

Tuning of the idler wavelength is achieved through varying the temperature (and therefore, the refractive index) of the non-linear crystal. Hence, in order to get stable and variable wavelength output, careful temperature control of the nonlinear crystal via thermo-electric cooling is necessary.

The OPO system [6,7] is optically pumped by a 3 W continuous wave (CW) laser diode operating at 808.5 nm. It is important that the wavelength output of the diode closely matches that of the absorption manifold of the laser gain medium. Therefore, it is again important to provide temperature stabilisation of this component, as the bandgap and hence output wavelength of the semiconductor diode is a function of its operating temperature. The operation of laser diodes is closely analogous to that of light emitting diodes (LED). As with the LED, a constant current supply is necessary for reliable operation. In this particular case a current supply of up to 3.5 A with a compliance voltage of 2.5 V is required. Therefore a supervisory system is required achieve this dual-channel temperature control (for the laser diode and nonlinear optical crystal) and constant current supply. A schematic diagram of the OPO components that require driving by external electronic systems is shown in figure 1.5 and an annotated photograph of the laser system is shown in figure 1.6.

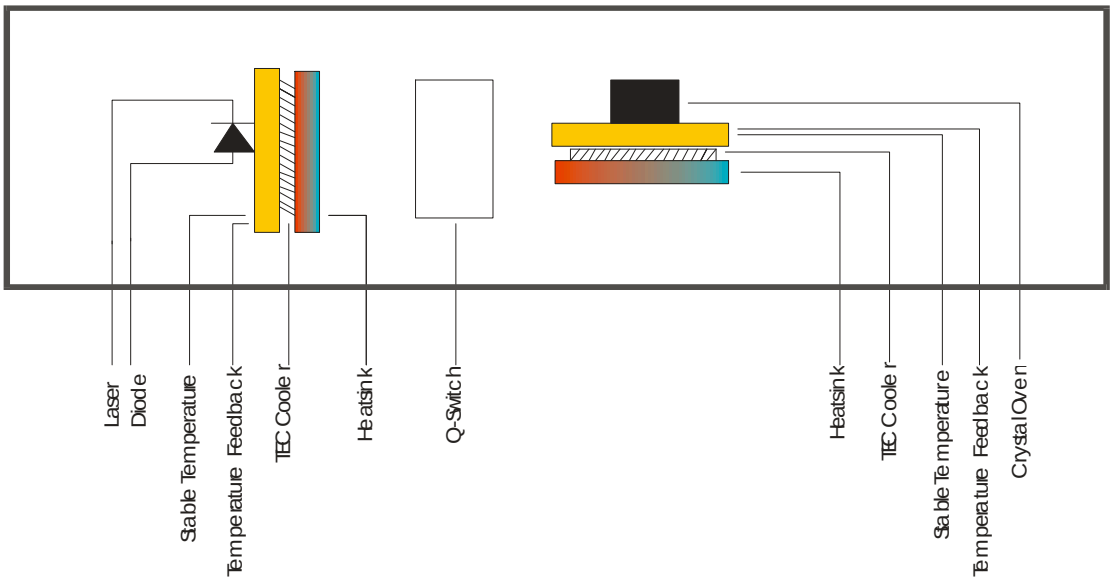

Figure 1.5 : Block diagram of OPO components which require electronic interaction.

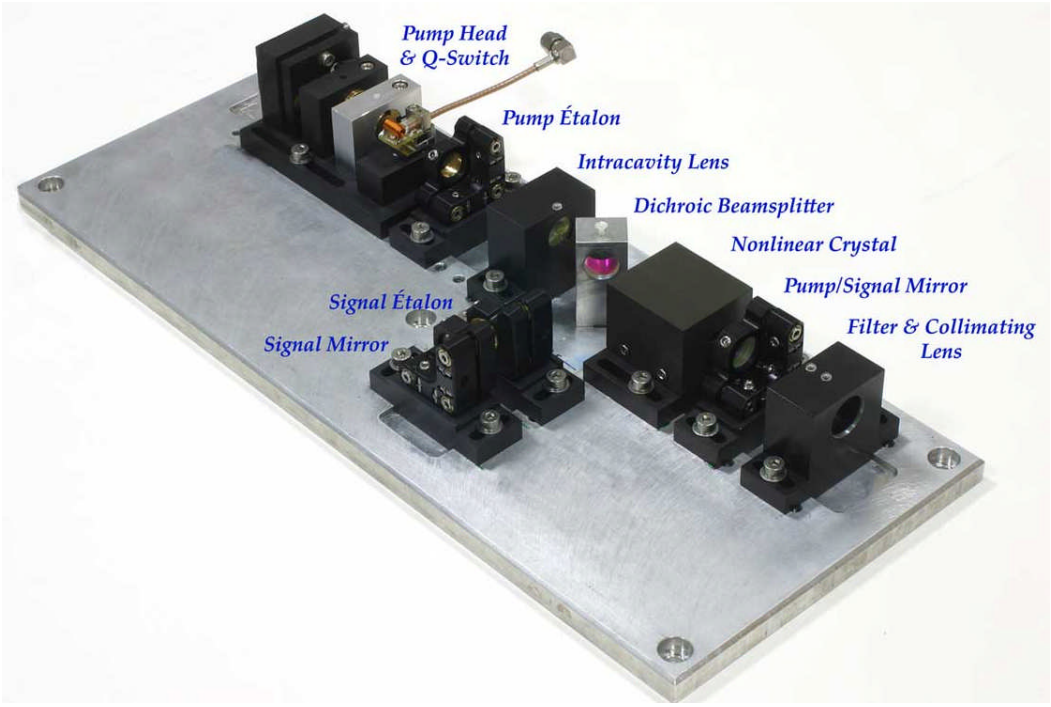

Figure 1.6: Photograph of the ICOPO system. The illuminating mid-infrared beam exits the system through the pump/signal mirror.

1. 4. 2 The Imaging System

With the illumination source for the BAGI detector sufficiently developed our attention now turns to the imaging system. A conventional imaging device utilises a two-dimensional video array of photodetectors to make a camera and for this application it might appear that a suitably sensitive mid-

infrared camera would be ideal. Unfortunately, cameras operating over this band, with sufficient sensitivity, are based upon mercury-cadmium-telluride (MCT) or Indium antimonide (InSb) arrays which require cryogenic cooling. Methods of cooling are either liquid nitrogen or miniature stirling engine heat pumps. These cameras are prohibitively expensive: approximately £50,000 per unit [8]. Such cost and complexity precludes the use of these cameras in this project. As such, an alternative image acquisition system is required.

This alternative is an electro-mechanical scanner based upon a rotating polygonal mirror and reciprocating galvanometer mirror. The idler beam is rapidly raster-scanned over the scene of interest and the amount of back-scattered light is collected and measured at each pixel point in order to build up the image. Such a system has the advantage of low cost (only a single element photodetector is required) and very good signal-to-noise ratio as each pixel point is measured with the full idler power incident upon it.

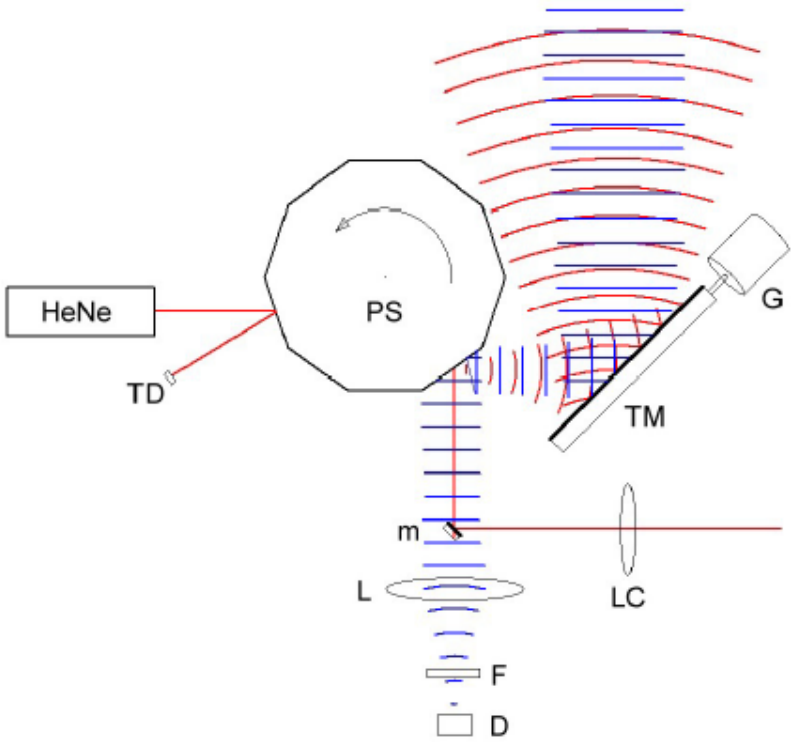

Figure 1.7: Polygon scanner schematic [9]

1.4.2.1 Polygonal Scanner

The geometry of the scanner used for imaging is shown in figure 1.7. Illuminating radiation from the optical parametric oscillator is directed along the optical axis of the arrangement by a small plane mirror **m** placed on-axis in front of the calcium fluoride collection lens **L** and then by the polygonal scanner **PS** which has 10 facets and tilting mirror **TM** to the scene under surveillance. The back-scattered radiation returning from the scene is collected via the same tilting mirror and polygon scanner and is then focused by the collection lens onto the MCT detector **D** located in the image plane of the collection lens. The area of the collection lens is sufficient such that the effective limiting collection aperture for the returned signal occurs at the polygon mirror facet. It is desirable to keep the area of the galvanometer mirror, polygon mirror facet and lens as large as possible in order to maximise the collected light and hence the subsequent measured signal. The above arrangement ensures that the detector always views that area of the scene currently being illuminated by the scanned idler beam from the optical parametric oscillator (i.e., the viewing direction is scanned in spatial synchronism with the illuminating beam). The calcium fluoride lens **LC** placed before the mirror **m** collimates the diverging idler beam. Since the MCT detector employed exhibits sensitivity over a broad range of wavelengths, a band pass filter **F** is placed in close proximity to the detector active area in order to reject stray infrared radiation from hot objects, laboratory lights and pump and signal fields that are leaked through OPO output mirror. A Helium-Neon or low-cost visible diode laser and detector **TD** are employed in order to trigger the image acquisition electronics at the correct point of the polygon rotation when scanning a horizontal line. A photograph of the polygon scanner mounted upon an optical bench is shown in figure 1.8.

A sample image acquired using this polygonal scanning system / OPO source, with the idler tuned into the peak absorption cluster in methane at 3.31μm, is shown in figure 1.9. In it the leaking gas is clearly visible. In it, the skin of the operator appears dark due to the high water content (and therefore absorption coefficient). It is also noticeable how dark the operators' spectacles are, demonstrating the need for optical components specially chosen for their high transmission properties in the min-infrared, for instance the calcium fluoride lenses.

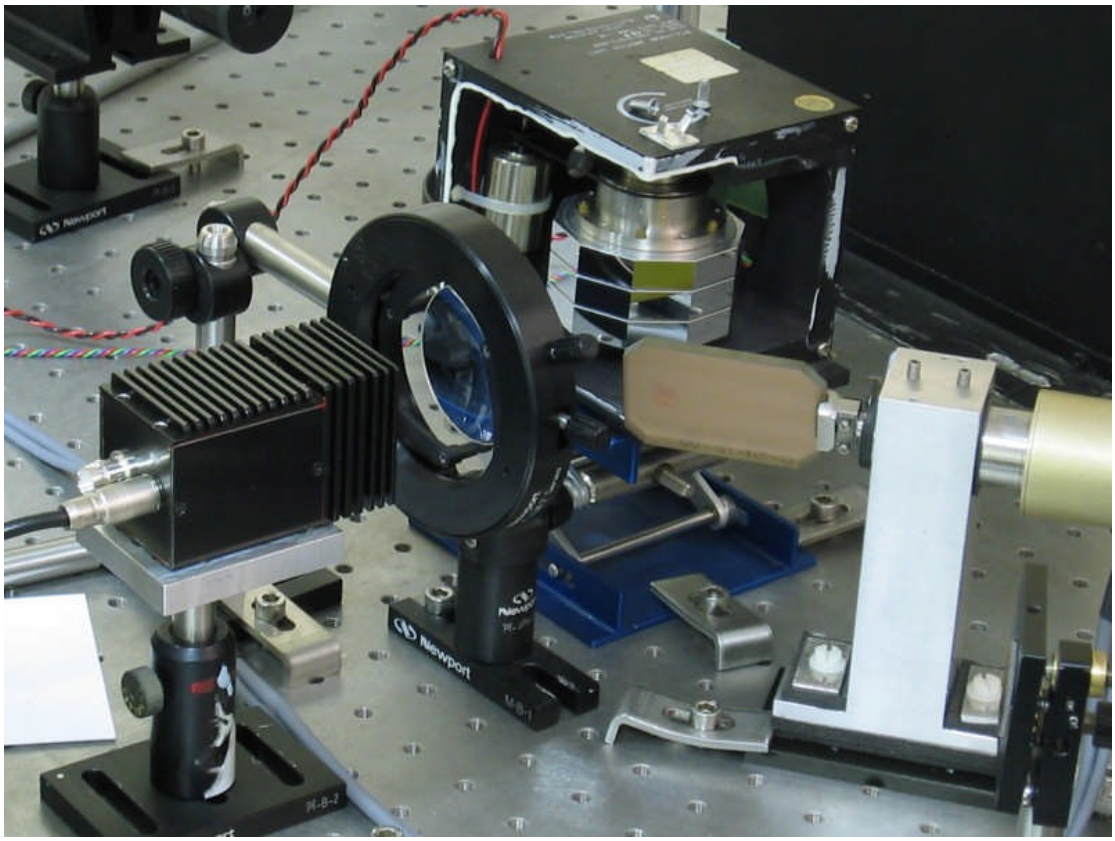

Figure 1.8: Photograph of the Polygon Scanner.

Figure 1.9: Sample image, acquired in the visible (left) and at 3.31μm using the polygonal scanner [9]

The imaging system scans the area under surveillance by means of an X-Y grid. The X component of the grid is controlled by the polygon and the Y component by the galvanometer. The grid comprises 150 horizontal samples by 100 vertical samples. The galvanometer scans both directions of the Y plane in order to save time by obviating the need to 'fly-back' the mirror. Figure 1.10 (a) highlights the order of sampling in the down direction with Figure 1.10 (b) showing the order of sampling in the up direction. It can be seen from this how vital time is saved by scanning in both directions. After the down scan is complete the galvanometer is already in position to start the up scan and vice versa

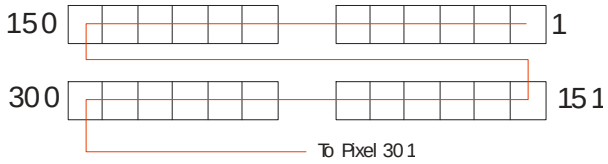

Figure 1.10(a): Order of sample acquisition in down scan

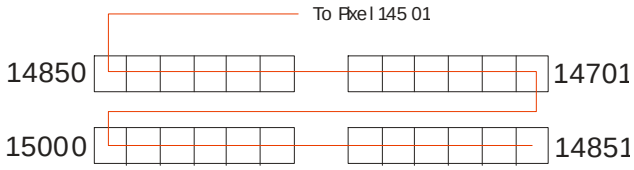

Figure 1.10(b): Order of sample acquisition in the up scan. Note the same direction of the x-scan due to the singular directional action of the polygon and the opposing direction of the y-scan due to the bi-directional action of the galvanometer.

At each pixel point, an optical pulse is emitted from the OPO, directed out into the scene of interest via the polygon and galvanometer, and its back-scattered signal is re-collected and focussed onto the detector where it produces an analogue signal. Areas with bright reflective type surfaces produce high signal levels and dark areas which exhibit high absorption produce lower levels of signal. methane has a very high absorptive properties with the OPO tuned to 3.31µm thus returning very low signal levels or indeed zero depending on the concentration of the gas. The analogue signal levels are converted to 8 bit digital values with 0 indicating the lowest detected signal and 255 indicating the highest. An analogue to digital (A/D) converter processes the signal into digital format. The sample data is stored into electronic memory and this data is continually downloaded onto a PC with specialist software to display the data in the X-Y image format shown in Figures 1.10 (a) and 1.10 (b).

1.5 Research Programme Outline

Such a scheme, whereby the image is acquired and stored in a bespoke electronic subsystem before uploading to a PC for display was acceptable in the infancy of this project, when the optical properties of the OPO were being investigated and optimised, but now this has been largely achieved it is highly desirable to remove the need for the host PC. This would be achieved by realising in-house designs for image acquisition, display driving and a high-resolution in-built LCD module for display. Such hardware will enable the eventual portability of the instrument for in-field testing. Also, during this initial research stage for the development of the OPO, discrete instrumentation was employed to drive the various components within the laser system. These included a Q-switch driver and associated signal generator, two separate temperature controllers for the nonlinear crystal and pump diode, a constant current source and various pieces of diagnostic equipment. Clearly, the portability of the scanner is severely compromised by the reliance of its illumination source on so many pieces of instrumentation. The second phase of this research programme, therefore, involved the realisation of a single driver device which could perform all of the functions previously described.

It is precisely the design and realisation of this electronic hardware, and the embedded microprocessor software upon which it depends is detailed in the following chapters.

Chapter 2 describes the early investigation undertaken to drive high resolution LCD displays. The two main display technologies available today, super twisted nematic (STN) and thin film transistor (TFT), are compared and contrasted for suitability for use within this project. Video driver integrated circuits are evaluated in the context of embedded processor control. Finally, the display technology of choice was integrated into a first prototype image acquisition system which had the capability to be interfaced to the scanning electronics developed prior to this project, or to be used as a stand-alone system.

The work undertaken in chapter 2 indicates the logical progression of the display and driver into a stand-alone module which had a RAM chip like electronic interface and could therefore easily be interfaced to a variety of microprocessor-based designs. In this way, the display driver technology could be perfected and easily produced and used in many different applications, not just restricted to

this one. The modular approach therefore split the design of the image display electronics into two main subsystems: the image acquisition (for control of the scanner electro-mechanical hardware) and the image display boards. The development integration and operation of these are described in chapter 3.

The design and realisation of the laser management system, which comprises a dual channel closed-loop temperature controller, constant current source and high repetition rate RF Q-switching system, is described in chapter 4. Here, the PID temperature control algorithm is described and a simple mathematical treatment is presented. The tuning of the PID loop for this particular device is also described.

The result of this research programme with be briefly summerised in chapter 5 and indications given into possible further avenues of work which would lead to performance improvements.

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Chapter Two – Data Acquisition and LCD Controller (DALC) System

2.1 Introduction

As outlined in the previous chapter, significant development work had already been invested in the development of the opto-mechanical polygonal hardware which makes up the scanning section of the BAGI device. In order to evaluate this hardware, an early supervisory electronic design was realised, in advance of the research programme outlined in this dissertation, which acquired pixel points and stored them in internal memory before uploading the data to a PC for viewing via custom-written software. This chapter outlines the early work undertaken in the course of this research in order to replace the existing electronic drive and host PC with a single device which integrates all of the scanning supervisory functions and high-resolution LCD display module and its associated drive electronics. Whilst the system described in this chapter had the capability of stand alone operation with control of the image acquisition hardware (polygon, galvanometer control and detector sampling as outlined in chapter 1) and display via the onboard LCD controller and high resolution display, we chose not to fully implement all of these features in this design. Instead, this early prototype was used to evaluate different options and technologies (for instance, the type of display technology used) for use in the finalised design as described in the following chapter. Therefore, the prototype design outlined in this chapter is more complex than the eventual final design necessitates. The opportunity for the evaluation of optimised track layout design for low noise analogue to digital conversion (ground starring, etc) was also undertaken in the device described in this chapter.

Instead of initially attempting to construct a stand alone module which both controls the opto-mechanical hardware of the scanner and the LCD display (which is the eventual desire), an interface was built in to the design which meant that the system could ‘mimic’ the operation of the host PC in the existing design and therefore interface to the existing image acquisition electronics. The two ways in

which the design described in this chapter, the “Data Acquisition and LCD Controller” (DALC) system could be implemented is shown in figure 2.1 below.

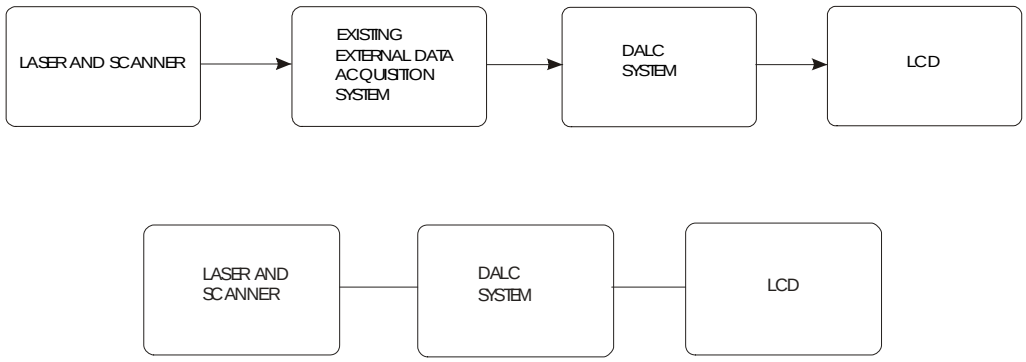


Figure 2.1: Implementation of the DALC system, which can either connect to the opto-mechanical hardware directly, or via the existing control electronics by mimicking the host PC which is currently present.

2.2 Data Acquisition LCD Controller System

This section gives a brief overview of the key components of the Data Acquisition LCD Controller system (DALC). A more detailed description of the hardware follows in the next section. The DALC system can process data for imaging from either the external data acquisition system currently in use or directly from its own data acquisition/hardware control. This capability was incorporated into the design to maximise its flexibility, it also allowed the image display hardware (graphic controller, LCD panel) to be assessed without the need to implement those parts of the circuit dedicated to image data acquisition (ADC,DAC laser trigger in etc). Such a modular approach to testing allows the rapid diagnosis of design flaws present within the system. The pre-designed system utilises a PC for image display via custom written windows based software.

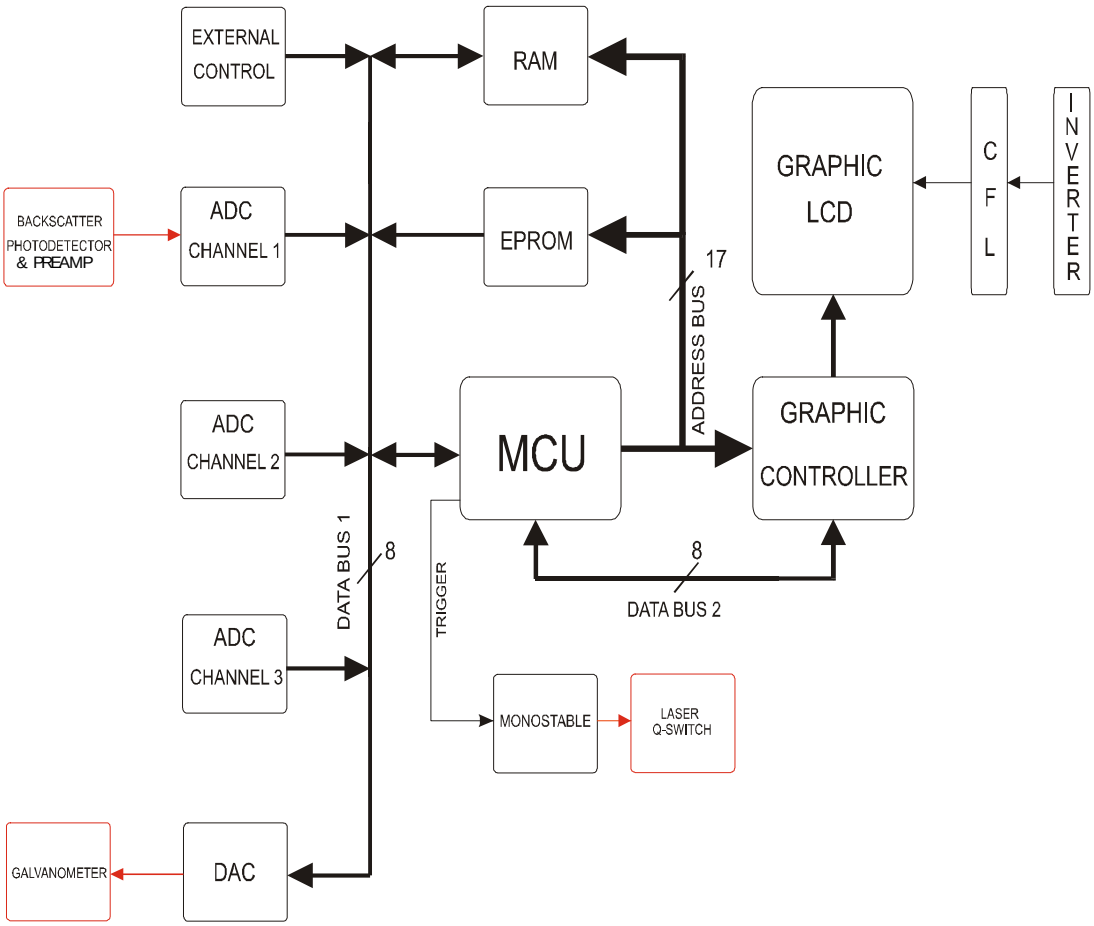


Figure 2.2 : Block diagram of DALC system (external components shown in red).

2.2.1Internal Data Acquisition

The hardware for the Internal Data Acquisition involves the ADC channels (for photodetector acquisition), the DAC (for galvanometer control), the RAM and the Monostable. These parts have been individually tested but have not yet been implemented as part of the Internal Data Acquisition, as the DALC system was superseded by a different design (chapter 3) before this became necessary.

2.2.2 External Data Acquisition

The external data acquisition system is configured for images of 150 x 100 pixel resolution giving one frame a total of 15,000 pixels. The laser is capable of firing at frequencies of up to 350 kHz however

due to limitations in the scanning hardware the maximum scanning frequency the system can provide is 120 kHz. This means that the maximum frame the system can produce is 120000/15000 which equals 8 frames per second. The DALC system is designed with specifications of 10 frames per second with the possibility of potential scanning hardware improvements. Data transfer between the existing scan acquisition system and the MCU takes place of an 8-bit parallel interface and is controlled by two handshaking lines; one controlled by the MCU which tells the external system the MCU is ready to receive more data and one which is controlled by the external system tells the MCU it is ready send data. When data is received by the MCU it addresses the Graphic Controller and writes the data to the corresponding address via data bus 2, which in turn asynchronously updates the LCD panel. To obtain a 10 frames per second refresh rate with the image being 150x100 pixels, this process would be repeated in excess of 150,000 times per second meaning the MCU speed capability is a major factor (actual bandwidth requirements are, in practice, in excess of 15,000 due to the tone-burst nature with which the laser fires and the photodetector signal needs to be acquired).

The hardware parts required for external data acquisition in conjunction with the existing scan system are as follows:

MCU	The MCU controls and synchronises the whole DALC system which can be seen by the following descriptions.
EPROM	The EPROM contains data from a greyscale bitmap to be used at system start up in order to obtain best image quality before the external data acquisition images had been tested. The bitmap image is a resolution of 256 x 256 pixels. The LCD panels being used are of 320 x 240 resolution and so the bottom 26 lines of the bitmap are not used.
RAM	Multiple image data can be stored in the RAM. The future requirements possibly being that two images of similar

	nature are stored and compared (differential imaging). The first image would be produced with the OPO being tuned at 3.31 microns and the other out with the methane absorption wavelength The second image would be subtracted from the first image leaving a third (differential) image being the methane. This methane image could then be modified in colour showing the intensity of the gas. This image could then be added to second image to show the background image in greyscale and the methane in a colour intensified image. This shows the need for the RAM to be capable of storing multiple image data. This process, however, requires improved design of the OPO in order for this to become possible and will be implemented in the future. The RAM can also be used in the internal data acquisition method.
➢ Graphic Controller	The graphic controller reads data from its internal RAM and converts it into signals required by the LCD panel. These signals vary depending on the nature of the LCD panel being used. The controller has to be configured accordingly for different panels; this configuration being implemented by the MCU writing data to various registers. Most LCD panels are required to be refreshed at (approximately) 70Hz which the graphical controller handles independently thus freeing up software overheads of the MCU.
➢ Graphic LCD, CFL and Inverter	The Graphic LCD panel produces the visual output for the DALC system. Most graphic LCD panels are transmissive meaning a panel backlight is required which is usually in

	the form of a cold cathode filament lamp (CCFL) with an inverter to drive the high voltage signal needed.

2.3 Micro-controller Unit

The microcontroller unit used in the DALC system is the dsPIC30F6014 manufactured by Microchip Technology [3.1]. The device is a 16 bit high performance microcontroller capable of 30 million instructions per second (MIPS). It was chosen for the following reasons.

- Fast speed – 30 Mips , sufficient for >10 frames per second refresh rate of the LCD panel.
- 16 bit data path allows for much quicker data transfer, processing and addressing within the system.
- 144 kB on chip program memory space allowing for major future developments.
- 8 kB of on chip RAM which will become useful in future when OPO techniques allow for differential image manipulation when small sections of data can be transferred into and out of this useful memory allocation.
- Easy programming via in circuit serial programming (ICSP).
- 84 user-selectable I/O pins allowing for freedom in design methods.
- Low cost in comparison to competitive MCU's.
- Future pin for pin compatible upgrades will become available with easy integration into current design.
- Easy code migration from previous microchip MCU's which previous experience and familiarity allows for quicker development.

2.3.1 Micro-Controller Unit Configuration

The dsPIC30F6014 requires a clock source which dictates the speed at which each instruction is executed. The MCU clock is configurable in a variety of ways and can easily be switched between different sources in software. The 10 frame per second refresh rate requires fast instruction execution

times to acquire data of 15,000 pixels per frame (at a resolution of 150x100 pixels). The source chosen for MCU clock is a 6 MHz crystal module and is programmed in such a way that this frequency is multiplied by 16 via an internal phase-locked loop to give an operating frequency of 96 MHz which is subsequently divided by 4 to allow the device to run at 24 Mips, yielding single instruction execution time of 42 ns. Fast clock sources require special RF considerations. For example, a 48MHz external clock could be multiplied by 2 internally by the on chip PLL to give the same results. The problem with this approach is that more careful considerations for RF and board layout are required to accommodate such a high frequency clock. So the best solution is to use a combination of a low external clock source and a high PLL multiple to achieve the desired result. The maximum PLL multiple on the device is x16. Although the MCU internal frequency runs at 96MHz it is designed with these considerations in mind to have little effect externally.

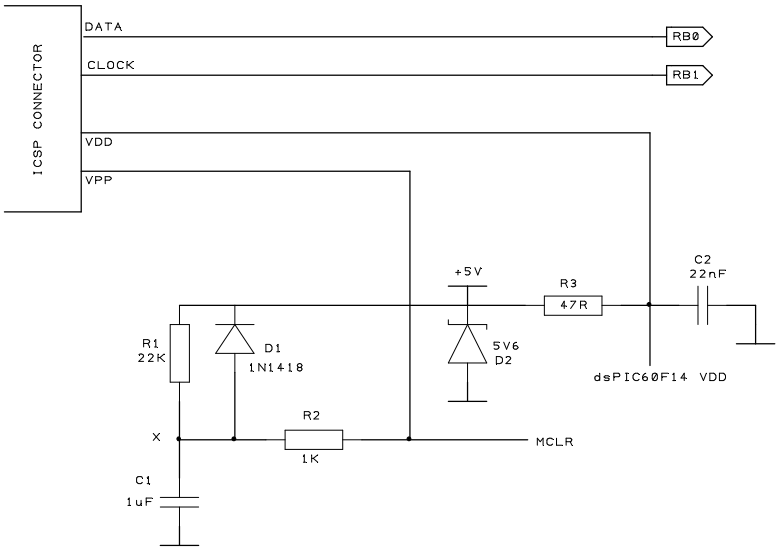


Figure 2.3 : MCU reset and ICSP schematic [2].

Figure 2.3 shows the reset pin and In Circuit Serial Programming (ICSP) circuit implemented in the system. The ICSP becomes necessary because the MCU is a surface mount device which is soldered directly into the system board and therefore is programmed in circuit as opposed to being removed from the circuit and being inserted into a programming device. The two programming lines CLK and

DATA are isolated from the system by the means of two 10 KΩ resistors. VDD has a decoupling capacitor to ground and the zener diode gives protection from spurious signals by clamping them at 5.6 V. R1 and C1 form the RC reset network to the MCLR pin with D1 giving protection at point x should it rise 0.6 V above the 5 V supply. Figure 2.3 shows how this circuitry was integrated into the system.

The dsPIC30F6014 has 84 easily configurable I/O pins arranged in various bit widths in the format of PORTA-PORTG. The I/O pins can have multiple functions, e.g. can be used for A/D input, PWM output, etc. This application of the MCU requires that all I/O used should be configured for straightforward digital I/O. Figure 2.4 shows how the I/O pins were configured for use within the system. The two sixteen bit ports available were selected for both 8 bit data busses and the 16 bit address bus. This was to speed up data transfer and addressing. The remaining allocation of the I/O pins were chosen with PCB design in mind allowing for shorter tracks and simplicity of board layout.

2.4 Graphic Controller

Very early on in the project it became apparent that direct control of the LCD display by the microprocessor would require a huge overhead in processing power, and would therefore not be practical. This is due to the non-static nature of the LCD module which continually needs to have each pixel point “refreshed”, regardless of if a change at a particular pixel point is required – somewhat analogous to dynamic memory. A dedicated LCD matrix controller was therefore procured which would enable much simplified interfacing of the microcontroller to the LCD display. The chosen device used for graphic control in the system was the S1D13706 manufactured by Epson research and development [3]. The main attraction to the device is its ability to produce 64 shades of grey on various panel types i.e. STN, TFT, D-TFT and HR-TFT. It’s on chip 80 Kbytes of video random access memory (RAM) make it adequate as a maximum of 76 Kbyte of RAM is required for the 320x240 panels used. The S1D13706 requires hardware and software configuration in order for it to be used successfully in the system. This section will cover hardware configuration and how the graphic controller was implemented into this system.

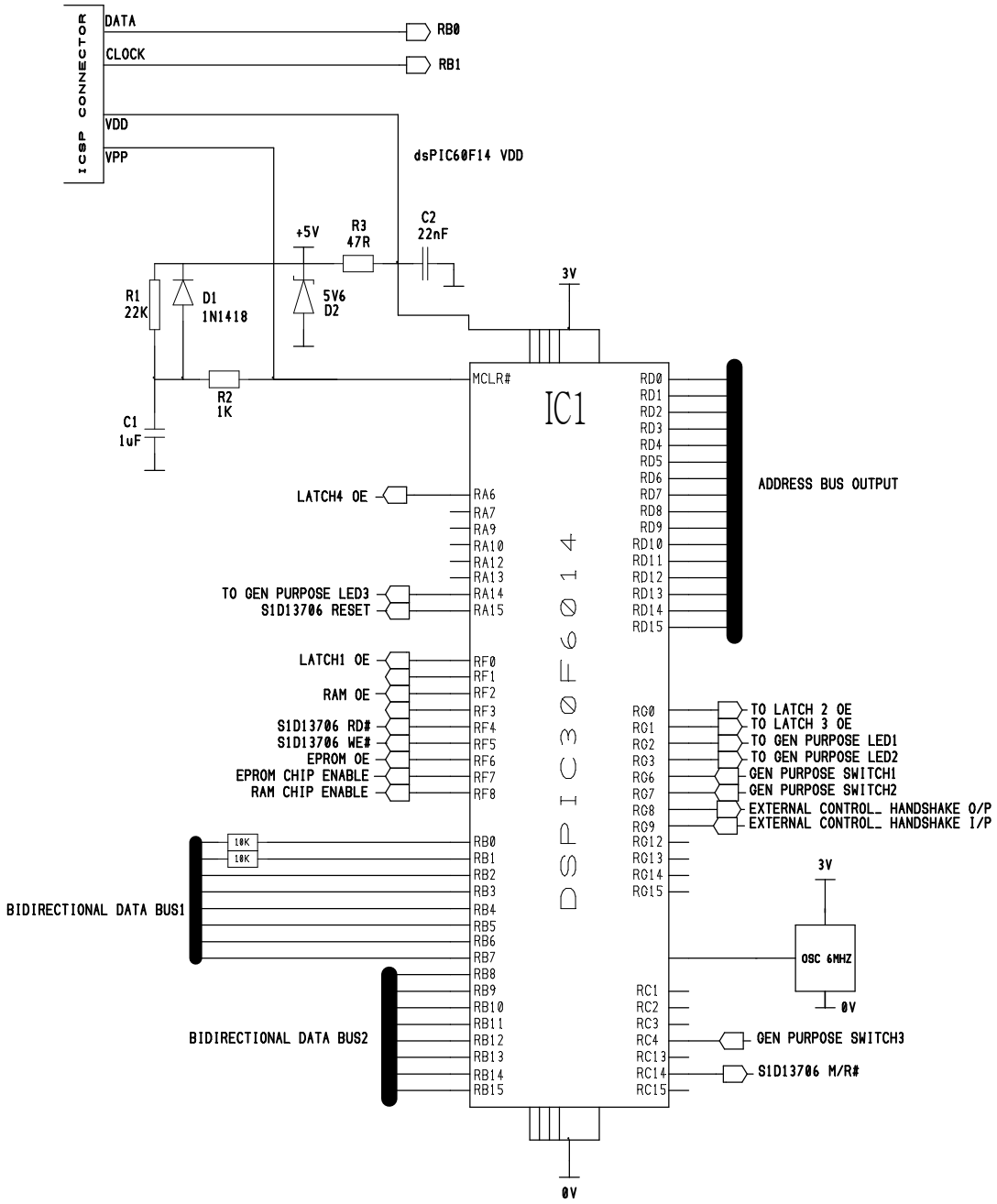


Figure 2.4: MCU clock circuit , Pin I/O configuration and ICSP/Reset circuitry

2.4.1 S1D13706 Bus Configuration

The device can be used with a host of microprocessors or microcontrollers and is engineered for ease of use with fast, powerful devices such as Motorola 32-bit 68030, Motorola 16-bit 68000, Motorola Dragonball, Hitachi SH3 and SH4 and many others. These devices are optimised for use in more demanding applications and can be embedded into single board computers. The device can also be

configured for generic bus interfacing to a microcontroller which is the method used within this system, in either 8 or 16 bit data transfer mode. The configuration chosen was 8 bit data transfer. Addressing of the graphic controller was configured by means of a 17 bit data interface to the MCU. The generic bus used is shown in figure 2.5. Bus start (BS#) and Read/Write (RD/WR#) are not used in the generic interface bus mapping and are tied to HIO/VDD. The memory mapping of the device is separated into two 128 Kbyte blocks, one of which is occupied by the internal registers and the other block is occupied by the 80 Kbyte display buffer. Pulsing M/R# high selects the display buffer memory and a low selects the register memory. Address bus 16:0 allows addressing to each of the 128 Kbyte of memory with the least significant bit of the bus selecting either the low byte or high byte of data, A0 low onto BHE# enables the high byte and a logic high enables the low byte. This is how 8 bit interfacing becomes possible. The RD# and WR# pins instruct whether data is read from the device or written to it. Reset to the graphic controller is controlled by an I/O pin enabling a software controlled reset.

2.4.2 S1D13706 Clock Configuration

The clock source used for the S1D13706 is a 50 MHz signal to the device is a crystal module that requires a 3 V supply across it. The device can be driven by one clock source as in this system or 2 clock sources. If two clock sources are used then the second clock source drives the output signals for the LCD panel directly and is optimised to derive the required frame rate for the panel – this source is the pixel clock (PCLK). The device has 4 internal clocks, bus clock (BCLK), memory clock (MCLK), pixel clock (PCLK) and pulse width modulation clock (PWMCLK) which can be used to output a PWM signal for backlight brightness control but is not required in this system as the inverter in this system has independent control. In this system BLCK, MCLK and PCLK were all derived from the CLKI source. The clock frequencies are all software configurable and were set as CLCKI = BCLK = MCLK = 50 MHz. PCLK=CLKI/8 = 6.25 MHz. Figure 2.6 shows the logical representation of the internal clocks and the registers required to modify them.

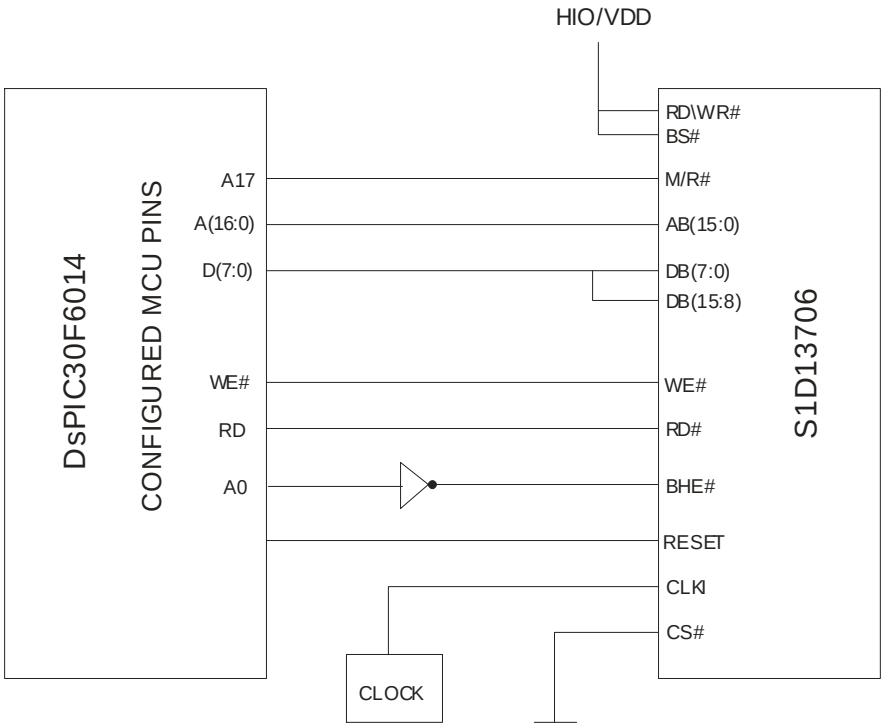


Figure 2.5 : Block diagram of dsPIC30F6014 and S1D13706 interface

2.4.3 S1D13706 Configuration Options

The S1D13706 has "power on" hardware configuration options which are shown in figure 2.7. The options available are selectable by 8 pins (CNF0-CNF7) set by external logic. The configuration required by the system are as follows.

- Generic #2 , Little endian
- CNF3 - doesn't matter. No output pins used.
- CNF5 – doesn't matter , wait state not required . Only required when MCU/MPU read write times < 5 ns as not to cause bus collision. The system MCU instruction cycle time is 42 ns.
- CLK1 to BCLK divide ratio 1:1 making BCLK 50MHz.

The logic levels are selected via PCB mounted configuration switches being connected to 0 V or Vdd. *Little Endian* and *Big Endian* refers to the way data is transmitted on a data bus. If 16 bit data had a value of 0xFEDC (hex) it would appear on the data bus as msb - FEDC - lsb. Big endian would appear

as follows, msb - DCFE – lsb. i.e. it swaps the bytes. This option is available because some MCU's or MPU's have different endian states.

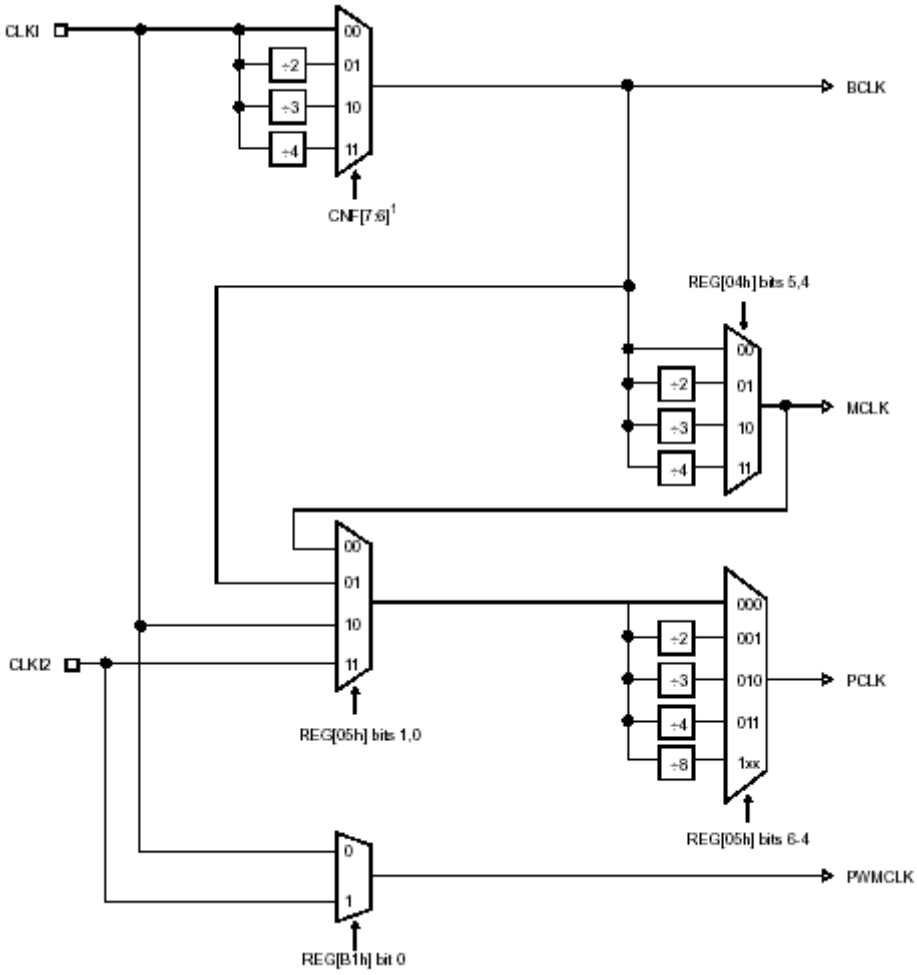


Figure 2.6 : Logical representation of the S1D13706 internal clocks

S1D13706 Configuration Input	Power-On/Reset State	
	1 (connected to $NIOV_{DD}$)	0 (Connected to V_{SS})
CNF4,CNF[2:0]	Select host bus interface as follows: CNF4 CNF2 CNF1 CNF0 Host Bus 1 0 0 0 SH-4/SH-3 interface, Big Endian 0 0 0 0 SH-4/SH-3 interface, Little Endian 1 0 0 1 MC68K #1, Big Endian 0 0 0 1 Reserved 1 0 1 0 MC68K #2, Big Endian 0 0 1 0 Reserved 1 0 1 1 Generic #1, Big Endian 0 0 1 1 Generic #1, Little Endian 1 1 0 0 Reserved 0 1 0 0 Generic #2, Little Endian 1 1 0 1 REDCAP2, Big Endian 0 1 0 1 Reserved 1 1 1 0 DragonBall (MC68EZ328/MC68VZ328), Big Endian 0 1 1 0 Reserved X 1 1 1 Reserved Note: The host bus interface is 16-bit only.	
CNF3	Configure GPIO pins as inputs at power-on	Configure GPIO pins as outputs at power-on (for use by HR-TFT/D-TFD when selected)
CNF5	WAIT# is active high	WAIT# is active low
CNF[7:6]	CLKI to BCLK divide select: CNF7 CNF6 CLKI to BCLK Divide Ratio 0 0 1 : 1 0 1 2 : 1 1 0 3 : 1 1 1 4 : 1	

Figure 2.7: Power on reset options [3]

Figure 2.8 shows the schematic of how the hardware of the S1D13706 was configured and the manner in which the S1D13706 was interfaced to the dsPIC30F6014. The outputs from the S1D13706 go to the LCD panel. The outputs in this system were connected to an IDC plug so any panel that the S1D13706 could drive could be connected to the system via a specific interface board designed for that panel.

2.4.4 Refresh rate calculation

Refresh rate of the LCD screen is calculated by the following formula where RR is the refresh rate, fPCLK is the pixel clock frequency, htotal is the horizontal total of the LCD panel and vtotal is the vertical total of the LCD panel.

$$RR = \frac{fPCLK}{htotal * vtotal} = \frac{6.25MHz}{320 * 240} = 81.4Hz$$

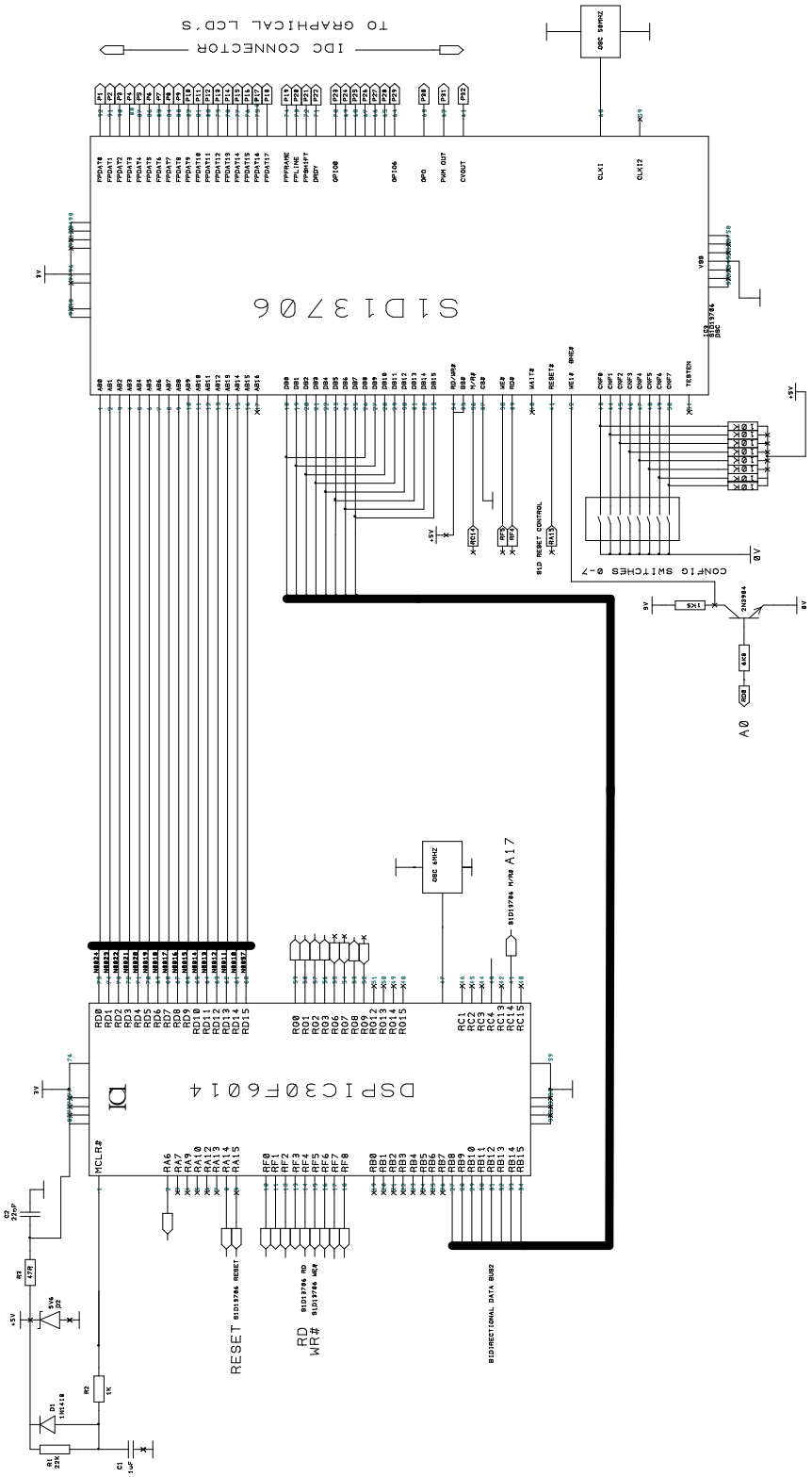


Figure 2.8 : S1D13706 hardware and MCU interface schematic

2.5 Analogue to Digital Converter Channels

The ADCs integrated within the microcontroller was not used as its maximum sampling frequency was inadequate for this application. Instead, three identical discreet analogue to digital converters with their own pre-amplification were used. They are based around the 8-bit analogue to digital converter ADS830 [6]. The device was chosen because of its high bandwidth capability, low distortion and high SNR ratio making it ideal for high bandwidth, low noise applications such as this. The device is capable of a 60 MHz sampling rate; significantly greater than the required 200 kHz required for a 10 frames per second refresh rate. However, possible future requirements make a higher bandwidth desirable. For example, one way to greatly reduce noise is to take a number of samples and then average the total and hence average out the noise. If 20 samples were taken the required bandwidth increases to 4 MHz , this could double should a 20 frame per second refresh rate be required and increase yet again if resolution was improved. This could therefore be implemented with ease into future designs.

The A/D requires voltage levels to be at a certain level and this biasing was achieved by the inclusion of an operational amplifier. The operational amplifier used in this design is an OPA2681 [7] which was chosen because of its high bandwidth – 150 MHz at 1-4 volts output swing and low noise low distortion capabilities. The OPA2681 is a dual current feed back device which enables the high bandwidth required. One op amp – IC1a drives the input of the ADS830 and the other – IC10b level shifts the signal to be compatible with the A/D input range. The RSEL pin is tied to +5V which allows a 2 Vp-p input range to the channel and the INT/EXT pin is tied to ground which means the device is using the internal reference (2 V). IC10b buffers the REFB pin from the potential divider R4 and R5 to give 1.25 V into the non inverting pin of IC1a giving the correct DC level of 2.5 V for the signal input (IN). The pins CM, IN, REFB and REFT are all bypassed with 0.1μF capacitors. It is important to note that everything described so far is connected to the analogue supplies with the ADS830 being treated as an analogue device. The voltage at the input (IN) will be converted and placed on the 8 bit data bus on every rising edge of the input clock which is selectable between OSC1 or RG13 of the MCU. This option is to free up software overheads by using OSC1 if required. The data is not transferred onto the main data bus until the output enable pin of IC3 is pulled low. The output of IC3 remains in a high

impedance state whilst the output enable pin is high allowing other devices command of the bus. When the data is on the main bus it allows the MCU to register the data via PORTB bits 0-7. Figure 2.8 shows the schematic of one of the A/D channels.

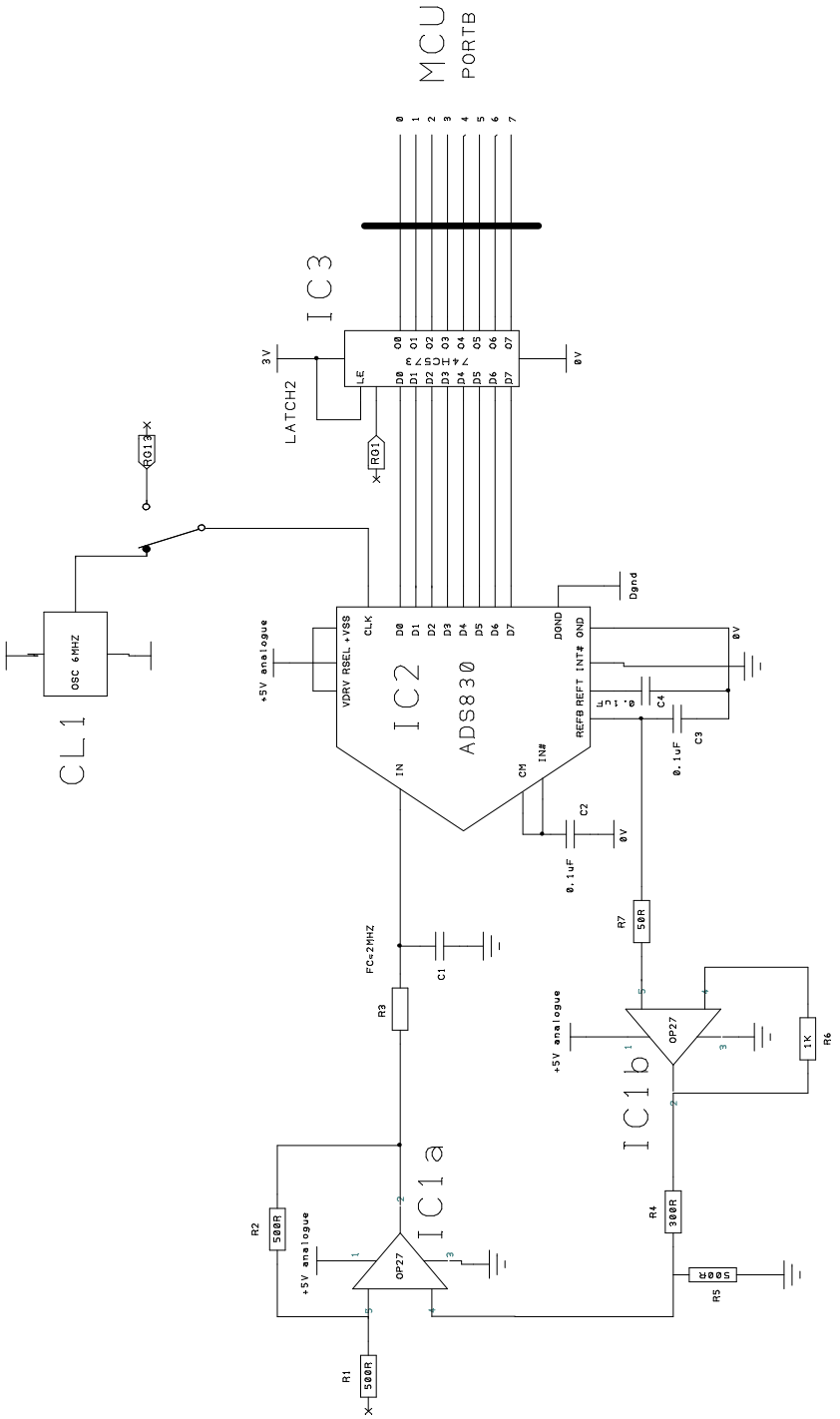
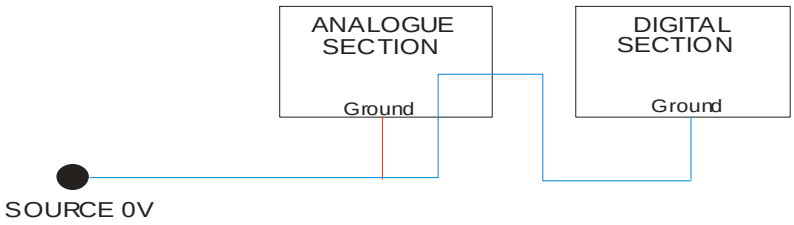


Figure 2.8 : A/D channel schematic with latch

2.5.1 Separating Analogue and Digital Grounds for Noise Reduction.

It is vital when measuring precise analogue data in mixed systems that ground paths have to be laid out carefully. This is because digital circuits generate a ‘noisy ground’ and this can lead to huge errors if this ‘noisy ground’ is the reference when acquiring sensitive analogue data. The solution is to separate analogue and digital ground paths and join them at a common point usually at the ground point of the power source (a technique known as starring). The ADS830 is treated as an analogue device with the digital part (the clock input and the data outputs) having its own ground for a separate return path so not to inject noise into the analogue part of the IC.

(a)



(b)

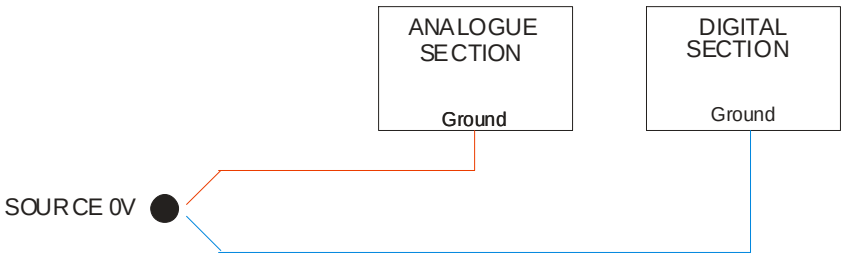


Figure 2.9 : Grounding options in a mixed signal system (a) Incorrect (b) Correct

Figure 2.9 (a) shows the incorrect method of grounding mixed signal circuits. The blue digital ground path passes directly through the red analogue ground path which therefore forces the analogue ground path to be of poor quality and hence analogue signals being converted will have a high proportion of error due to the digital noise. Figure 2.9 (b) shows the correct method. Both sections have their own return path to the source 0V so the analogue ground is isolated from noise generated by the digital ground.

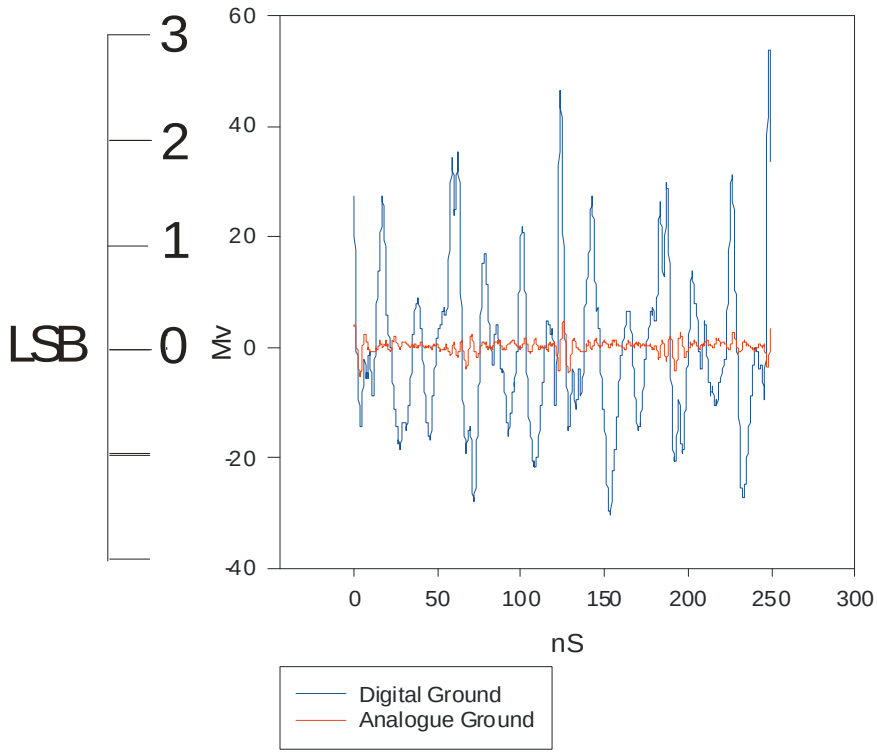


Figure 2.10: A comparison of noise present in the digital and analogue grounds.

The two traces from Figure 2.10. are measured from the two 'separated grounds' on the system. It can be seen that the analogue ground is of a much better quality than that of the digital ground. However if the ground paths were connected as in diagram 2.9 (a) then both grounds would be of similar magnitude i.e. Digital ground. The analogue ground has a magnitude of approximately 8 mV p-p whereas the digital ground has a magnitude of approximately 90 mV p-p thus minimising any errors whilst sampling the analogue signal. This low level noise ensures no least significant bit (LSB) errors occur whereas at 90 mV the resultant error could be as much as 4 LSB's making measurements very inaccurate.

2.6 Digital to Analogue Converter

The digital to analogue converter (DAC) used in the system (included to provide the analogue positional drive signal for the galvanometer) is an 8-bit AD7801 from Analog Devices [8]. The data appearing from the bus appears on the high speed parallel input of the D/A. The device is configured in such a manner that it is updated on the rising edge of WR. This is done by permanently tying the LDAC pin low. The reference of the device is generated internally and is configured by tying the reference pin permanently high. By selecting the internal reference the output of the device is Vdd/2. The clock into the WR# pin is again selectable between OSC1 and RA9 to allow for the possibility of reducing software overheads if required. The DAC output was tested by applying a 1.5 Vp-p AC signal into an ADC channel, with the latch output enable pulled low to allow the converted data to appear on the bus. This data therefore appears at the DAC high speed parallel input. Both the ADC and DAC are driven by Clock 1. On every rising edge of Clock 1 data is converted to its analogue output. Figure 2.12 highlights the distortion between the input analogue signal and the output analogue signal. The output signal is still of acceptable magnitude being only 4mV p-p which is well within the least significant bit error of 19 mV. Better considerations to ground layout and increasing track thicknesses for the supply lines (to reduce inductance) should suppress these peaks further. Figure 2.11 shows the schematic of how the D/A converter was integrated into the system and tested with an A/D channel.

2.7 EPROM

The EPROM used for the static image “test screen” was a 27C512 [9]. It was chosen because of its ease of programming and its ability to store 64KByte of data. This allowed for the bitmap image of 256x256 to be stored on the IC (256x240 displayed on panel). Once programmed the device is easily controlled by enabling the OE# making the data outputs high impedance state to free up the bus or by disabling the pin for the data to take command of bus. Another control input to the device is the CE# which when enabled switches the device to a low power standby mode. Both these lines are controlled by the MCU. The EPROM shares the sixteen LSB’s of the address bus and when the two control lines are disabled the data stored on the corresponding address appears on data bus 1. Figure 2.13 shows the

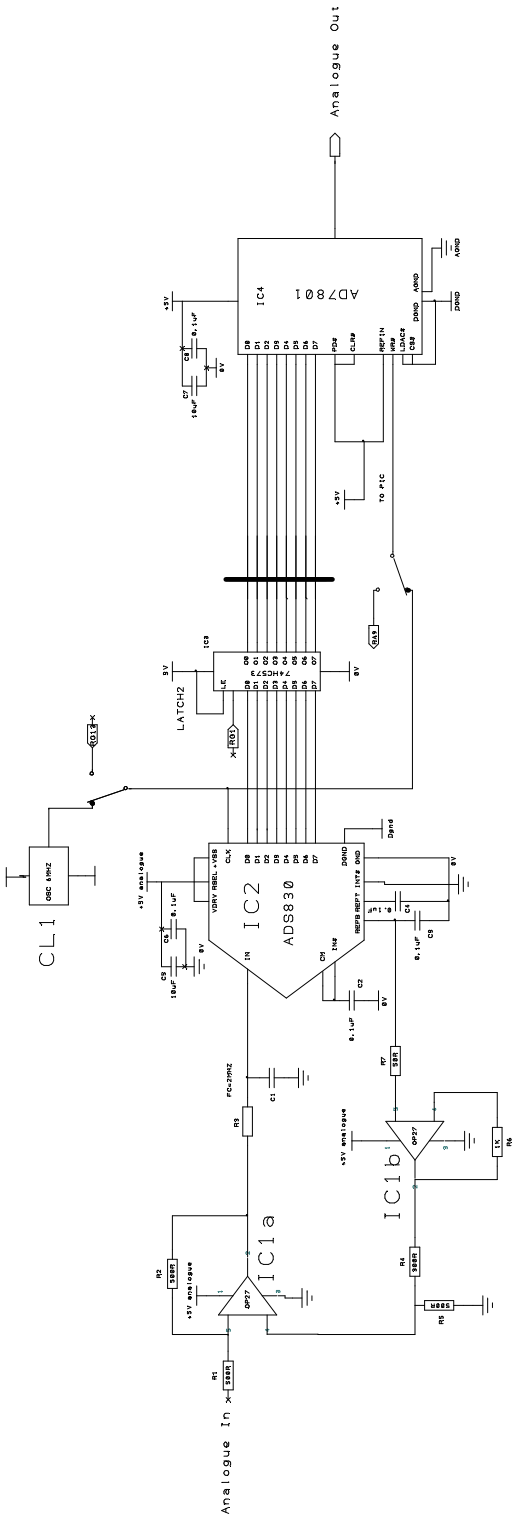


Figure 2.11 : D/A schematic and system integration

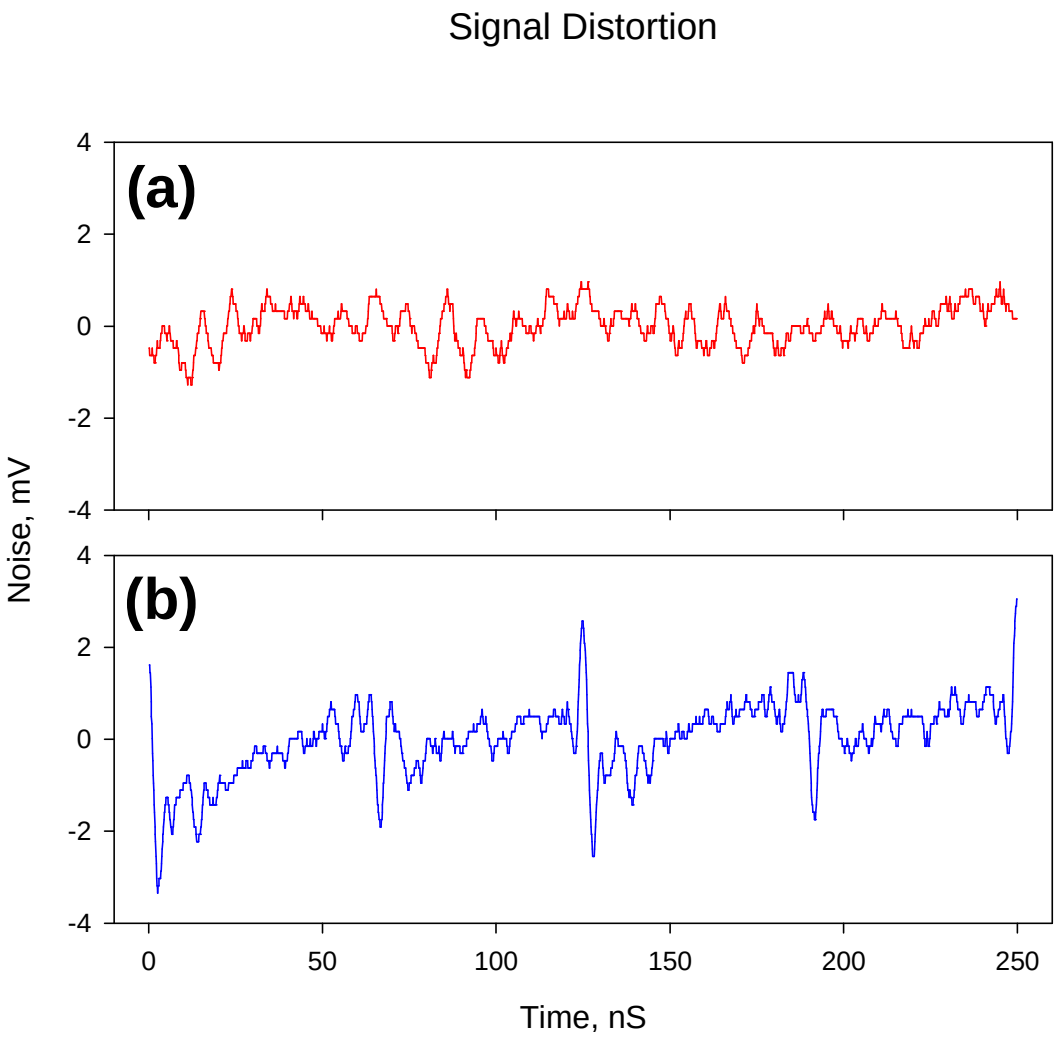


Figure 2.12: Distortion of signal (a) before and (b) after being processed via A/D then D/A

256 greyscale PC bitmap image that was programmed onto the EPROM. The image of General Kitchener, an instantly recognisable black and white image, was chosen specifically to highlight the greyscale quality of the black and white display and also its high resolution. The 256 shade greyscale bars highlight this with the gradual blending from black to white. This image, stored at a bit depth of 8-bits (i.e. 256 shades of grey) will be rendered on the screen in 64 shades of grey due to the limitations of the LCD module and the graphics IC. Reduced bit depth can lead to "postarisation" where smooth gradients are quantised into blocks of tone and the grey graduate strips were included in the image to facilitate evaluation of this effect in the use of these displays. The limitation of 64 shades of grey comes about due to the intensity resolution of the RGB components within the display module. Each red, green and blue pixel point has only 6-bit (i.e. 64 level) intensity resolution. When used as a colour

display, this yields a palate of 18 bits (262144 different colours), but when used as a black and white display (when R=G=B) this falls again to only 6-bit intensity resolution, hence 64 shades of grey.

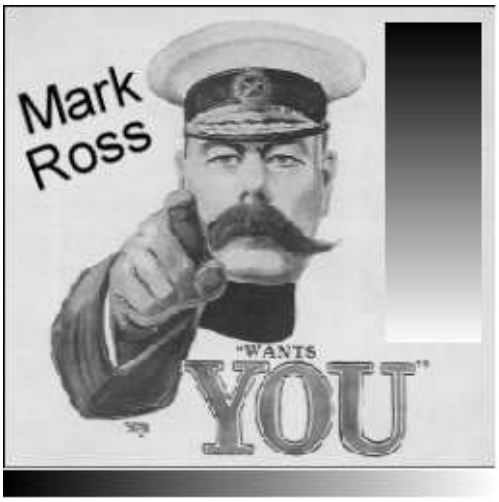


Figure 2.13: 256 greyscale test bitmap image

2.8 Random Access Memory

Random access memory (RAM) is included in the system in order to buffer the incoming data stream if necessary, and also for the storage of multiple frames for the purposes of differential imaging. Incorporating RAM on the board is not strictly necessary as the microcontroller is fast enough to stream the incoming data into the LCD control chip in real time. The memory was included on the board at this time for evaluation purposes and also to enable the possibility of implementing the aforementioned differential imaging technique, where two (or more) frames are acquired at different illumination and them simple comparisons between them are made in order to highlight the positions within the image which correspond to the presence of methane. The RAM used in the system is a BS62LV4001SC-70 manufactured by BSI semiconductors [10]. The device is capable of storing 512 Kbytes of data which allows for multiple image storing for data manipulation with each image on this system requiring 15 Kbyte. The RAM operates in a similar fashion to the EPROM with an additional control line for putting the device into either read mode write mode which is again controlled by the MCU. The write mode requires a low input. The RAM also has 4 additional address lines, 17 from the address bus and an additional 3 to access the full 500 KByte of memory.

2.9 LCD panel, CCFL and Inverter

There are two major types of LCD array technology available today. Passive matrix displays and active matrix displays. Both types were tested in the system for performance comparisons and each have 320x240 pixel resolution. Although at this stage both panels are tested in 64 shades of grey they are capable of producing colour and this capability will be exploited if differential imaging were realised. The passive matrix display tested in the system was the SN14Q001 [4] from Hitachi. The active matrix display tested in the system was the TX14D11VM1CBA [5] also from Hitachi.

2.9.1 Basic Passive Matrix Operation

In passive matrix displays a glass substrate imprinted with rows forms a liquid-crystal sandwich with a substrate imprinted with columns. Pixels are defined at row-column intersections. To activate a given pixel, a timing circuit energizes the pixel's column while grounding its row. The resulting voltage differential renders the liquid crystal opaque in the vicinity of that pixel location, blocking light from coming through. This technology is older than that of active matrix displays and suffers from significant disadvantages. The largest drawback is that Super Twisted Nematic (STN) panels have slow screen refresh rates which can result in "ghosting" images when fast moving images are required. This would seem inappropriate for the system because of the specified 10 frames per second refresh rate required. Also edges can become blurred in passive matrix displays because the voltage at matrix crossover points can affect surrounding pixels stopping light from flowing through. This affect can have a degrading effect on contrast. Figure 2.14 shows the EPROM static image being displayed with the DALC system on the STN panel.

This image has poor contrast although the edges appear reasonably sharp. To test the STN panel refresh rate capability a test procedure was introduced using the DALC system. The procedure involved refreshing the static frame so that when a new frame appears every pixel is shifted one place to the left which gives an animated image moving from right to left.

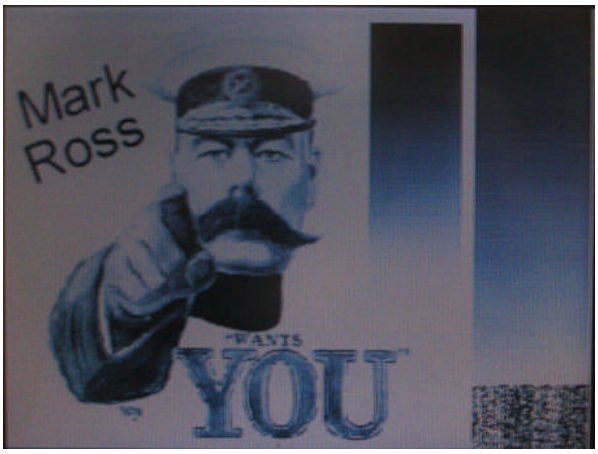


Figure 2.14 : Eprom image displayed on STN panel

The refresh rate of the static image was 10 frames per second. Figure 2.15 shows part of the image zoomed in during this procedure and it can be seen that he edges become very blurred producing a poor quality image. The camera shutter speed used to obtain the image was less than the scan refresh rate.

Figure 2.15 : Animated image produced with the DALC system on the STN panel showing poor dynamic performance

2.9.2 Basic active matrix displays

The active matrix display tested in the system was the TX14D11VM1CBA. Active matrix displays (also known as TFT – thin film transistor) use more modern technology and are now the fastest selling

LCD technology due to much improved performance compared to STN which in turn has driven massive price drops making them even more popular. Active matrix displays are manufactured with IC technology. Each pixel has a transistor switch manufactured into the glass and a capacitor to hold the charge between refresh rates – typically 70 Hz. A pixel is addressed by applying a voltage to its column via a and enabling its row by applying a transistor gate voltage allowing only the required pixel to be affected and not neighbouring ones, thus enabling much sharper edges. Less current is drawn in driving a pixel resulting in much faster refresh rates. For colour displays such as the one used in this system each pixel has three sub pixels producing red green and blue, which the human eye just perceives as one pixel. The 320x240 TFT panel used actually has 230,400 pixels (3x320x240). Each sub-pixel has 6 intensity levels making the display 18-bit colour. The number of colours possible from the TFT display is 64 x 64 x 64 = 262,144. The TFT panel can display 256 out of the 262,144 possible colours simultaneously using the S1D13706 graphic controller. This is done by software control programming a look up with up to 256 entries of RGB data. To display the data the location of the look up table is accessed. Figure 2.16 shows the EPROM static image being displayed with the DALC system on the TFT panel. Figure 2.17 shows a zoomed in image of the image being animated with the same procedure used for the STN animation. The quality difference can be clearly seen with the sharp contrast and particularly the sharp edges in the animated image in comparison to the STN panel output. The blue tone on the figure is an artefact of the white balanced used on the digital camera used to photograph these images and was not perceptible under normal viewing conditions. It is worthy of note that although this image is rendered in only 64 shades of grey, there is virtually no perceptible evidence of postarisation in the gradient areas of the image. This is perhaps as much due to the limitations of the human eye in differentiating between very small changes in tone as it is to the quality of the displayed image.

2.9.3 CCFL and Inverter

Industrial type panels of the physical size used in the system require high intensity light for the panel's backlight. Smaller TFT panels such as the ones used in mobile phones require much less light power because of the small active area and LED's can be used for them. The backlight used for the selected panel requires a cold cathode filament lamp which isconstructed behind the panel. CCFL's are glass

tubes with electrodes at both ends. The gas is pressurized neon mixed with mercury. When mercury becomes electrically excited it produces ultra-violet light. The UV optically excites the phosphor coating which in turn relaxes and radiates visible light in the process.

Figure 2.16 : Eprom image displayed on TFT panel

Figure 2.17 : Animated image produced with the DALC system on the TFT panel (note clarity of image features)

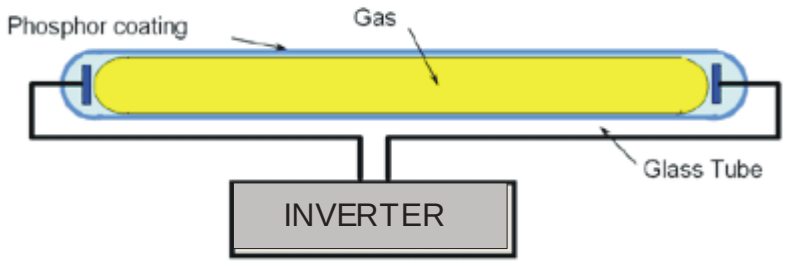


Figure 2.18 CCFL diagram [14]

CCFL's require a high striking voltage of typically 1000 Vac to ionize the mercury. When this occurs the voltage drops to a lower voltage of 500 Vac. To achieve this an inverter is used which requires a 5 V input. The inverter uses a feedback circuit which ramps up the high voltage until the CFFL strikes. The inverter used is INVC617 [13] recommended by Hitachi for use with the TX14D11VM1CBA.

Figure 2.19 shows the schematic of how the display and associated components are interfaced into the system. The 18 bit data lines are connected to the panel 6 blue , 6 red and 6 green. The two other data lines are required for the timing signals. One line is to inform the panel when each new frame begins (DTMG) and the other is the clock signal to input the 18 bit RGB data for each pixel. The S1D13706 reads data from its RAM and converts the data into the required signals for the configured panels. It also handles all the timing of these signals for the correct operation of the panel which makes the actual operation of the LCD panel largely transparent to the MCU, significantly freeing up processing power.

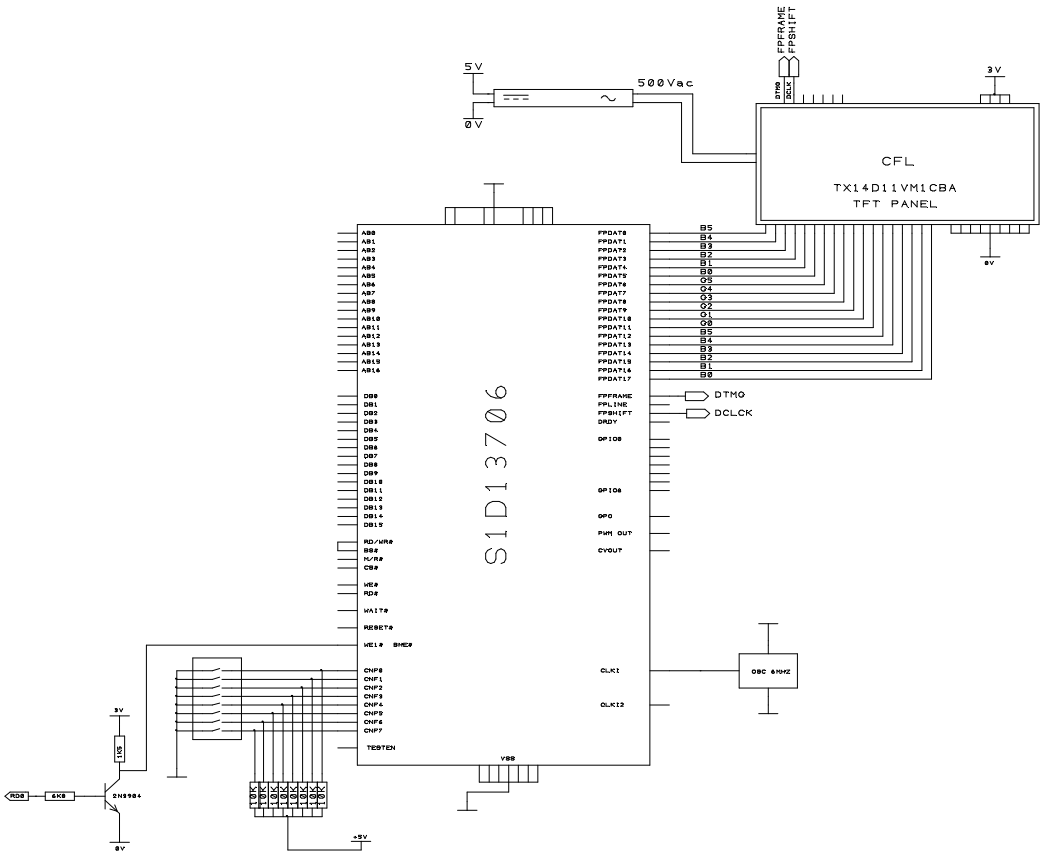


Figure 2.19 display integration to S1D13706

2.10 External Data Acquisition Interface

Figure 2.20 shows the interface for feeding data from the external data acquisition into the DALC system. The handshaking line RG8 controlled by the MCU tells the external system that it is ready for more data transfer. The external system is computed around a 5 V core with the DALC system around a 3 V core. Therefore voltage level shifting is required for correct compatibility. The 3 V handshaking line (RG8) from the MCU is level shifted at the transistors collector to 5 V at the collector of TR1. This signal is inverted from the 3 V which is not a problem because software can compensate for this. The handshaking line from the external system which tells the DALC system (via MCU pin RG9) that it is ready to transfer more data is shifted from 5 V to 3 V by means of a simple voltage divider. The 8 bit data bus is also transformed by this means with each data bit being passed through a potential divider.

Any data appearing here can be transferred onto data bus 1 by means of setting the LE# input of the data latch (IC2) to a logic level high allowing data to be then processed my the MCU.

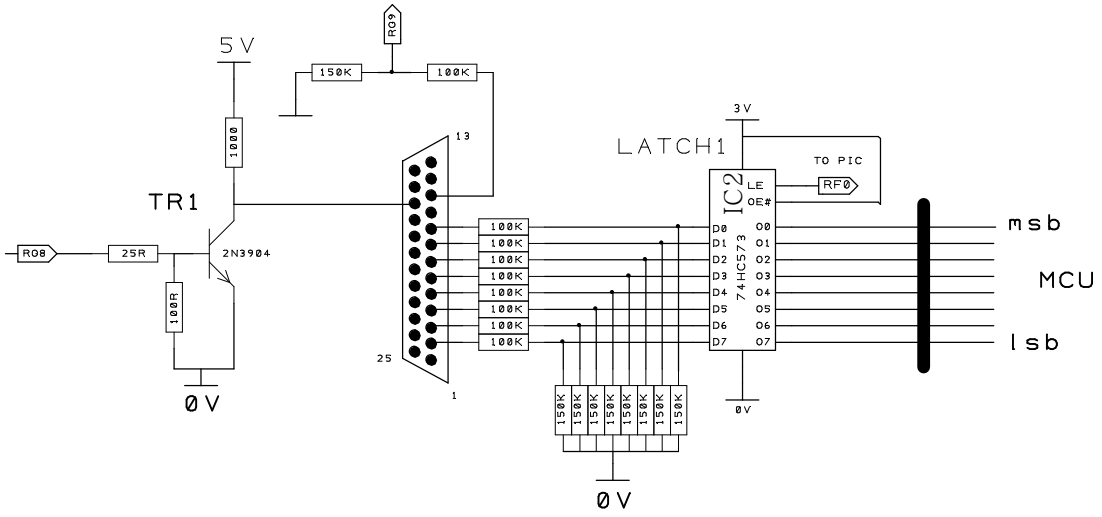


Figure 2.20 : External data acquisition interface

2.11 Software Control

The dsPIC30F6014 is a microcontroller with a Digital Signal Processing engine for fast math operation. It can be coded and compiled by either using a 'C' compiler or it's own assembly language, which boasts many improvement on previous MCU's in the Picmicro family while maintaining easy migration. The new, more powerful instruction set allows for faster execution code speeds. The system was programmed in dsPIC assembly language to avoid the time efficiency penalty incurred by C programs. The system code requires no floating point maths (just simple integer adding and subtracting) therefore assembly is the best choice. The flowchart for the system operation is shown in Figure 2.22. A full listing of the assembly code is included in the appendix, and the enclosed CD-ROM.

The first task of the program is to configure I/O ports. This is set up in initial states as to avoid any bus collisions. For example, the data latches are tri-stated on the data bus as are the EPROM data outputs and PIC data bus outputs etc. The single control lines for the system are either configured to input or outputs as required. The next task is to blank the LCD panel before configuration, this is to enhance the life of the LCD panel as directed by the data sheet. The firmware has to decide which LCD panel to

configure, the TFT or STN, depending on push button one being pressed (STN configuration) or not (TFT configuration). The 64 bit greyscale is then configured by writing to the 256 bit lookup table. Since there are 256 locations in the lookup table in the S1D13706 memory and 64 shades of grey to display, the method of allocating the grey shade to the lookup table is such that grey value 0 is allocated to lookup table memory locations 0-3, grey value 1 is allocated to memory locations 4-7 and so on. Once the lookup table is configured the bitmap image on the EPROM has to be displayed. This is done by accessing the EPROM address 0x00 and writing the stored data into the S1D13706 buffer memory at location 0. This is done until address 256 is reached then since the panel is 320x240 and the bitmap image is 256x240 the firmware writes the EPROM address 256 at the S1D13706 buffer address of 255 + 80 to display the data on the next line of the panel. The firmware then waits on push button 2 being pressed to activate image upload from the data acquisition system. For uploading the image the first upload is in the up direction then the down direction etc. This acquisition is determined by uploading a line at a time. The DALC sends a signal to the acquisition system that it is ready to accept data. The data for one line is then uploaded into the DALC system which then sends an acknowledge to indicate it is ready for another line of data. When the last line is loaded then the direction changes to a down scan. The DALC system is capable of 10 frames per second at 256x240 resolution although the firing laser is capable of only 6 frames per second. The reason for the remaining frame rate is one of forward engineering for such circumstances of if and when the OPO evolves to take advantage of the higher frame rates. Figure 2.21 shows a bitmap image capture with the greyscale test screen it has overwritten shown to the right of the bitmap frame. A listing of the firmware code for this chapter and all subsequent chapters appears in appendix B. For the sake of brevity, a line-by-line description of its (and subsequent firmware code) functionality will be omitted. Figure 2.22 shows a simplified flow chart of program flow.

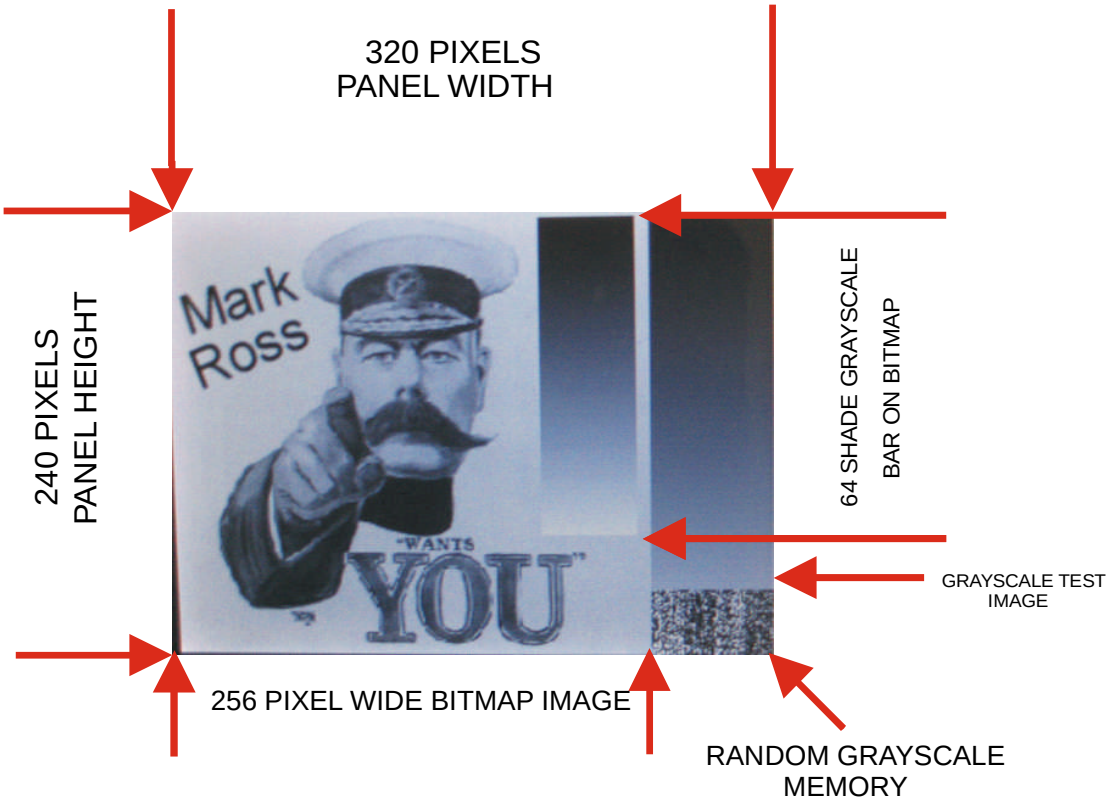


Figure 2.21: Image capture with 256x240 bitmap

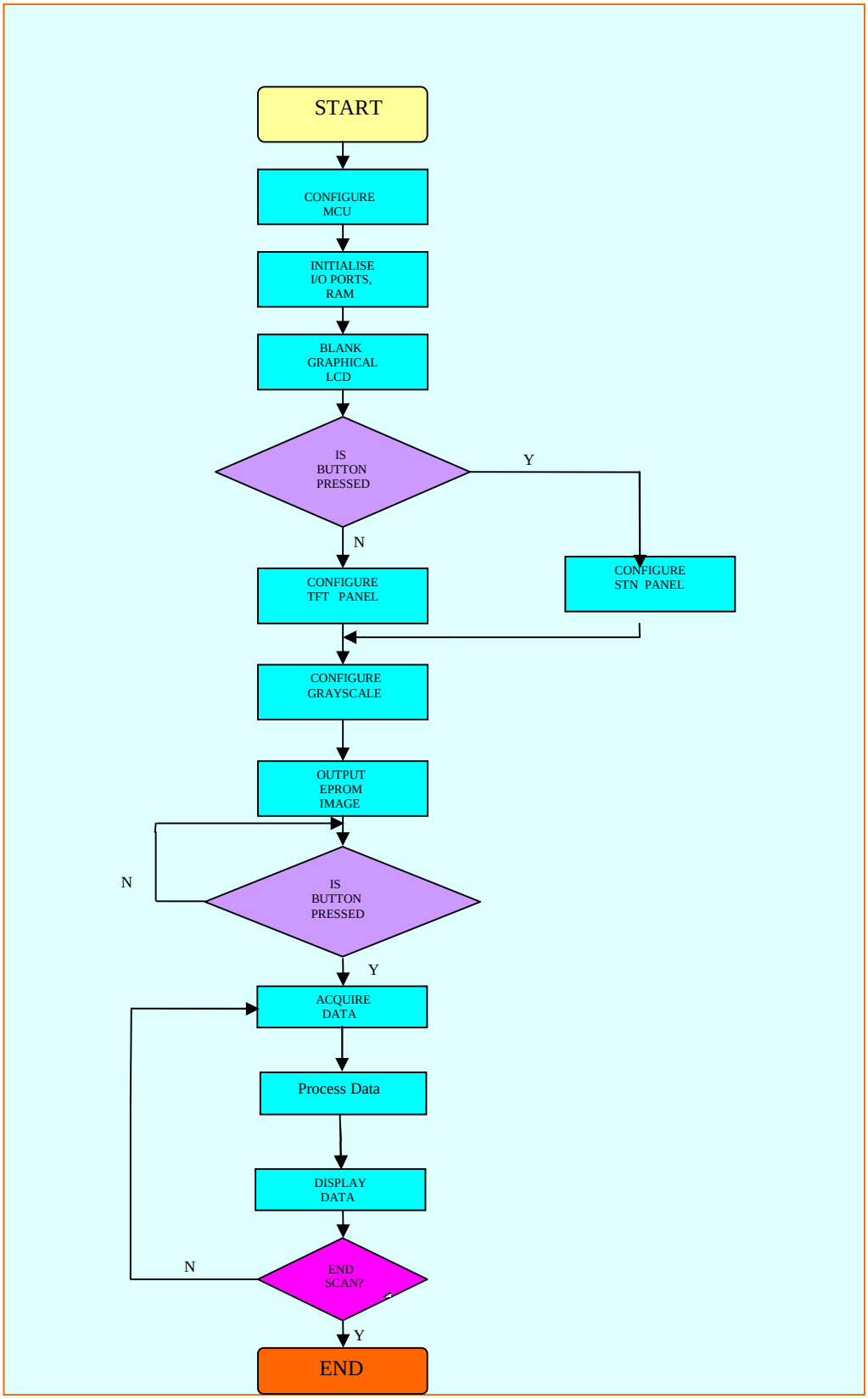


Figure 2.22 : Flowchart of system operation.

2.12 Chapter 2 Results

The chosen clock frequency and execution speed of the MCU of 96 MHz and 42 ns seconds proved adequate in this current design for the screen refresh rate of 10 frames per second. The graphic controller used in the system produced excellent results with the versatility of driving both STN and TFT displays and thus allowing for the conclusion that the TFT display was far superior to that of the STN in terms of overall quality in displaying both static and animated images. As figures 2.23-6 show

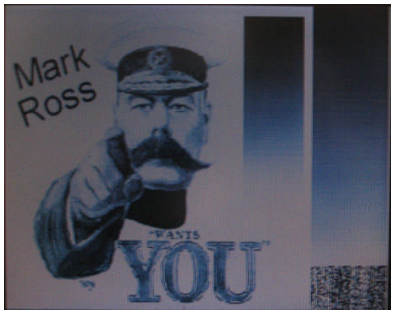


Figure:2.23 Static STN

Figure:2.24 Static TFT

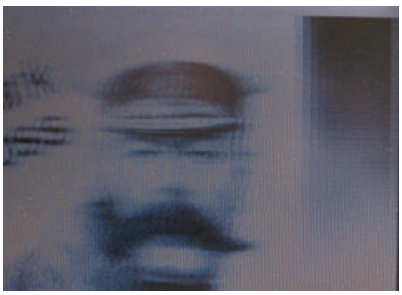


Figure:2.25 Animated STN

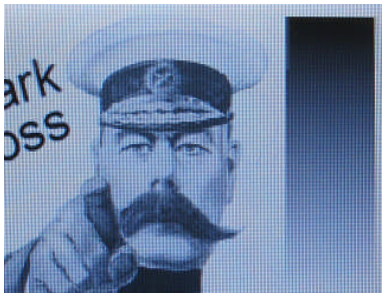


Figure:2.26 Animated TFT

The core of the system, the MCU, proved to be an excellent choice for a variety of reasons. The execution time was more than sufficient as previously said and also the factor of the vast number of configurable I/O pins allowed for flexibility in the circuit design and also the PCB layout design. The fact that the device was indeed 16 bit allowed for faster addressing and data transfer instead of 8 bit data transfer and thus helping to achieve the target of 10 frames per second. Also, the fact that previous

experience has been obtained on the Microchip family of MCU's, the easy migration to the dsPIC30F6014 enabled vast time investment in learning a new product family.

The ADC, DAC and RAM were operationally tested successfully however it was decided that these optional components would play no part in the evaluation of the system. The low noise grounding techniques of the ADC and DAC however will prove useful throughout the course of this research.

The use of the EPROM implemented into the system for holding data for an introduction screen proved a success in terms of ergonomic value as well as a great resource for debugging purposes. Figure 2.27 shows a picture of the DALC system displaying the EPROM.

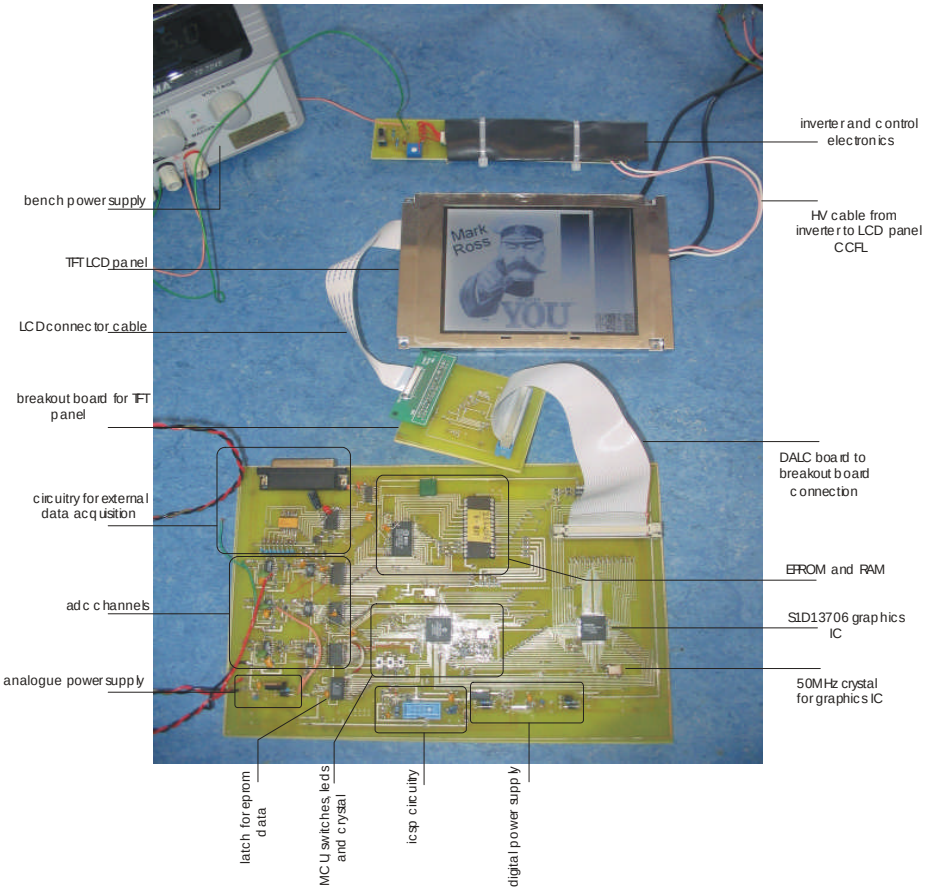


Figure 2.27: Photograph of the DALC system

2.13 Summary

In this chapter a prototype image acquisition and display system was developed, and its many subsystems evaluated. The system developed was designed to be as flexible as possible so that different options for the finalised design could be explored and optimised. The system featured multi-channel ADC channels, a DAC channel and RAM for acquisition of the back-scattered video signal, control of the vertical galvanometer and storage (and potential manipulation) of the acquired image. Each of these subsystems were tested for use in a future design, although they were not used in unison to realise an integrated stand-alone image acquisition system. Real time images acquired by the scan hardware were however displayed by interfacing to the existing image acquisition electronics previously developed.

The most significant development during this section of the research programme was the realisation of integrated LCD control hardware, and successful interfacing and control of a high resolution LCD display, thereby obviating the need for an external PC for image display.

With the design, test and evaluation of the DALC system the research in chapter 2 will realise a new imaging system utilizing the tried and tested components used such as the MCU, the graphic controller IC, the TFT flat panel display and the EPROM.

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Chapter Three: Image Acquisition Display (IADD) System & Random Access LCD System (RAL)

3.1 Introduction

Work in this chapter was carried out in collaboration with Dr. David Stothard, School of Physics and Astronomy, University of St. Andrews to whom I extend my gratitude.

It was realised during the development of the system outlined in the previous chapter that a more versatile, modular approach to system design could be implemented and would be highly desirable in the context of maximising the potential use of the display technology developed during the current and future research programmes. We therefore decided that the results and expertise gained from the work described in chapter 2 could be used to design a more versatile standalone LCD display system with technology that could be easily interfaced in a simple manner to connect to a variety of imaging systems and be used for general purpose fast access graphical purposes. By placing the image display hardware on a single board with a very simple digital interface, the LCD could be driven by a host of devices even if those devices featured only very modest computing power. Such a modular approach results in two principle subsystems to the overall image acquisition hardware electronics; the image acquisistion and display sub-modules. The idea was that these two individual systems can be incorporated to become one small and easy to operate instrument for use within the detection system. These two individual systems described in this chapter are the image acquisition & display driver (IADD) system and the random access LCD (RAL) system.

3.2 Data acquisition display processing system (IADD)

The data acquisition display & driver processing (IADD) system was developed with the aim of improving over the current pre-designed data acquisition system used to drive the DALC board in the previous chapter. The new system is designed with more versatility and is capable of driving a stepper motor as well as a galvanometer for y-deflection of the illumination beam. The huge advantage of a stepper motor drive is one of cost (more than an order of magnitude cheaper), and therefore we decided to integrate a dedicated stepper motor driver to evaluate this option. The IADD system is capable of driving both the new Random Access LCD (RAL) system described later in this chapter in section 3.3, and a PC via its parallel port, either together or individually. The improved architecture of the new system over that realised before the onset of this research programme generates an X-Y format allowing for faster frame rates as well as higher resolution images to be acquired due to the larger random access memory (RAM) of 128 Kb. Dual in line switches are included to allow for real time modification of the acquisition parameters such as resolution and system timing. As in the previous design, the analogue signal from the single-element photodetector is amplified and converted to a digital signal by an ADC. This data is written in a memory location, all of which is synchronised by the MCU. The LCD display interface appears as a standard RAM chip to the supervising MCU and indeed its interface simply sits in parallel with the onboard memory, therefore placing no overhead in the required MCU processing power. Data is presented to it in a cartesian x-y format (for pixel positioning) on the Ram chips' address bus, and the pixel grey-scale shade is dictated by the data on the data bus. This data and position is clocked in to the LCD module by the RAM chips _WR_ pin. The LCD display therefore places no overhead whatsoever on the host MCU.

When connected to a PC for image upload and storage, the image data is read back from the onboard RAM and is sent to the PC over an 8-bit parallel interface with two handshaking lines, as outlined in the previous chapter.

3.2.1 Components of the IADD system

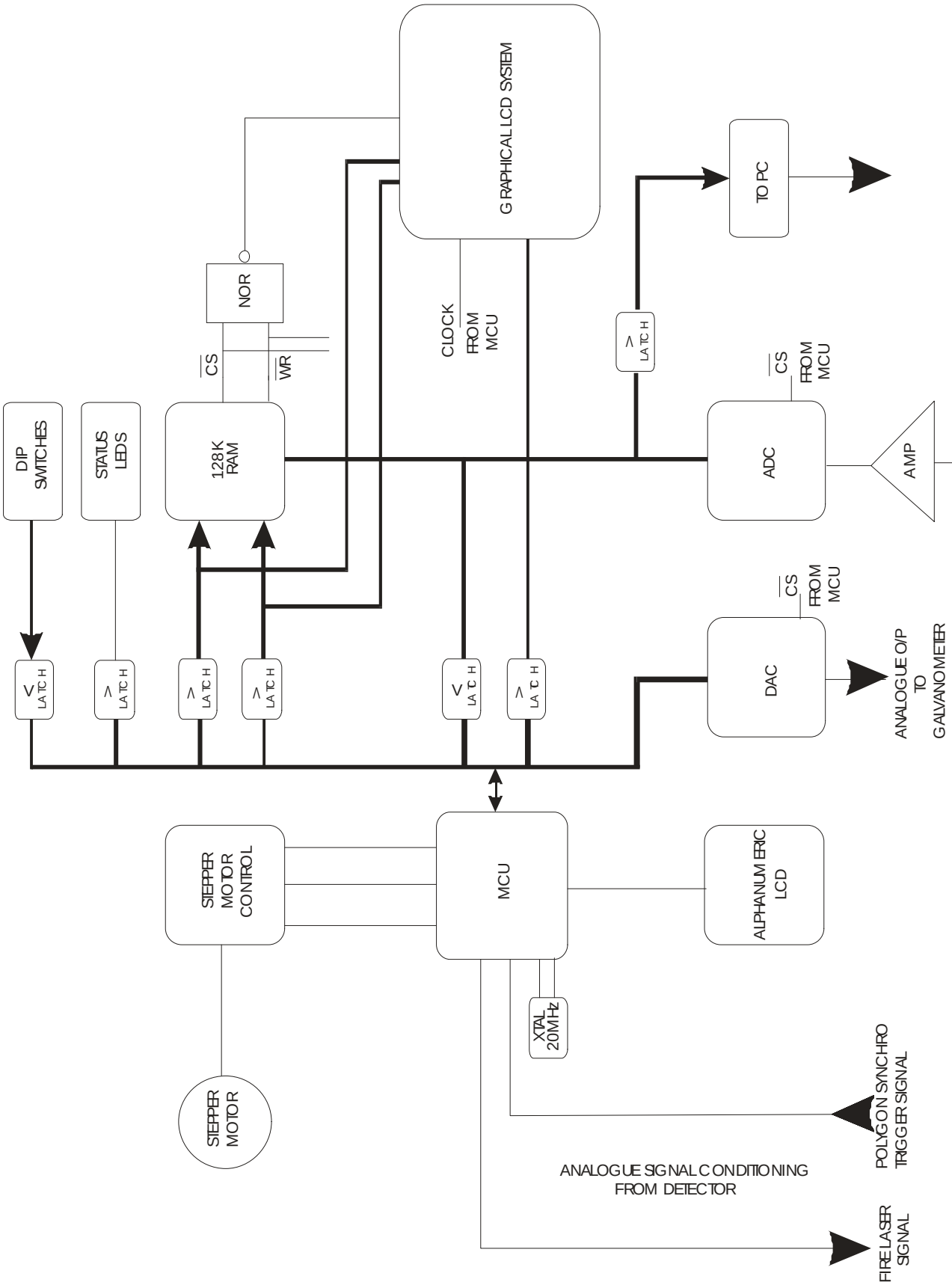

Figure 3.1.: Block Diagram of the IADD system

The following table outlines the key concepts if the IADD and their functions.

MCU	The MCU synchronises and controls all the data flow and manipulation within the IADD system.
RAM	Acts as a buffer of data transfer between the IADD system and the PC. Not required when only using the RAL display module, which features its own video RAM.
Stepper Motor Controller	Controlled by the MCU, the stepper motor controller drives the stepper motor by applying the required signals to the motors coils and providing sufficient drive current.
Stepper Motor	Used for scanning in the Y direction as an alternative approach to the galvanometer.
Alphanumeric LCD	Used for user feedback and debugging purposes.
DAC	Used to convert digital signals to an analogue equivalent to control the galvanometer for scanning in the Y direction.
Amplifier	Signal from the detector are amplified and offset to appropriate and sufficient levels for use within the system.
ADC	Data from the amplifier are converted to 8 bit digital format for manipulation and transfer by the MCU.
LATCH	Present to transfer data to and from the two busses with synchronised timing by the MCU.
Status LED's	Used to show system status and for debugging.
DIP Switches	Used to configure different settings with the system, such as resolution and acquisition timings without the need to reprogram the MCU.
PC	A PC can be connected to the system for viewing and saving scanned images.
RAL (Described in section 3.3)	The RAL system is a modular viewing system designed for use with the IADD system but with the versatility to be controlled and driven by many other systems.

Figure 3.2: Table of IADD component functions

3.3 Micro-Controller Unit

The microcontroller unit used in the IADD system is the 16F874 manufactured by Microchip Technology [1]. The device is a lower end device in the Microchip family of microcontrollers and is capable of 5 million instructions per second (MIPS). Even though this device is a low-end MCU it was chosen because although there is a series of complex switching and timing considerations there are no large memory or ultra fast speed requirements. An important factor in the choice of this device is that there are pin for pin compatible upgrades available. Device highlights are:

- Reasonable speed of 5 MIPS giving an instruction execution time of 200 ns.
- Adequate memory – 4K flash memory and 192 bytes of data memory.
- 33 I/O pins for multiple control ability.
- Low cost in comparison to competitive MCU's.
- Pin for pin compatible upgrades available if required.

3.3.1 Micro-Controller Configuration

The data flow is broken down into three separate busses: The general purpose bus (GPB), the data bus (DBUS) and the latched address bus (LAB). The GPB handles signals such as RAM address, DAC data, DIP switch status etc. The DBUS handles the flow of data between the ADC, RAM, LCD Display and the PC interface. Note that although the contents of the DBUS are available to the microcontroller via a dedicated data latch, this is not normally required and the microcontroller shunts the contents of the DBUS between the ADC and RAM without actually requiring access to it. The design was separated in this way to increase speed by decreasing the number of op-codes needed to be executed as each pixel point is sampled. The use of separate address and latching buses was implemented due to the requirement of the device to access 64k (i.e. 16-bit) of memory space, and for this to be achieved without the fully-functional hardware address mapping control pins which are present on a classic microprocessor, such as the Z80.

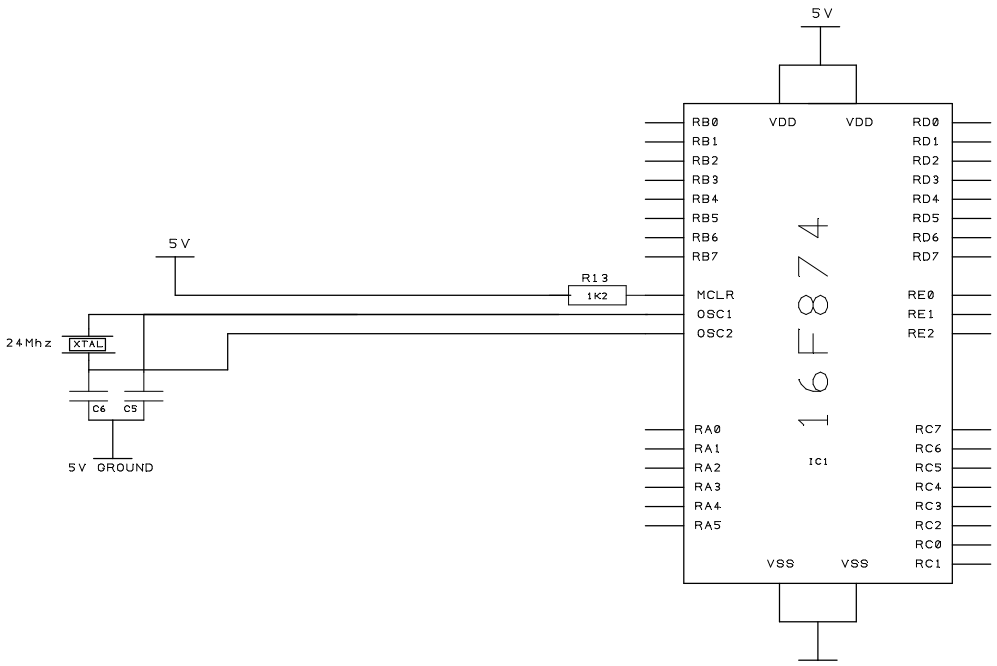

Figure 3.3: Diagram of basic MCU hardware setup (Clock & Reset)

The MCU is powered from the 5 V logic supply. The MCLR pin is pulled up to 5 V to give a hardware reset at switch on. The system clock for the MCU is derived from a 20 MHz crystal XL 1. This crystal has two load 15 pF capacitors connected from each pin to ground with both pins connected to OSC1 and OSC2 of the MCU with OSC1 being the oscillator input and OSC2 being the oscillator output (see figure 3.3).

The MCU controls and synchronises the data to and from the general purpose bus (GPB) to the other two busses which are the latched address bus and the data bus with the aid of data latch integrated circuits – 74HC573 [2]. The data latch IC's have eight data inputs and 8 latched outputs along with 2 control pins, latch enable and output enable. The devices work such that the data on the inputs are latched onto the device with a high to low transition of the latch enable pin. This data will appear on the latched output pins if the output enable pin is low – however if the output enable pin is high the data is disabled from the output pins which go into a tri-state mode allowing for other data to take control of the bus. The bus data transfer then work as follows.

3.3.2 Micro-Controller and bus control

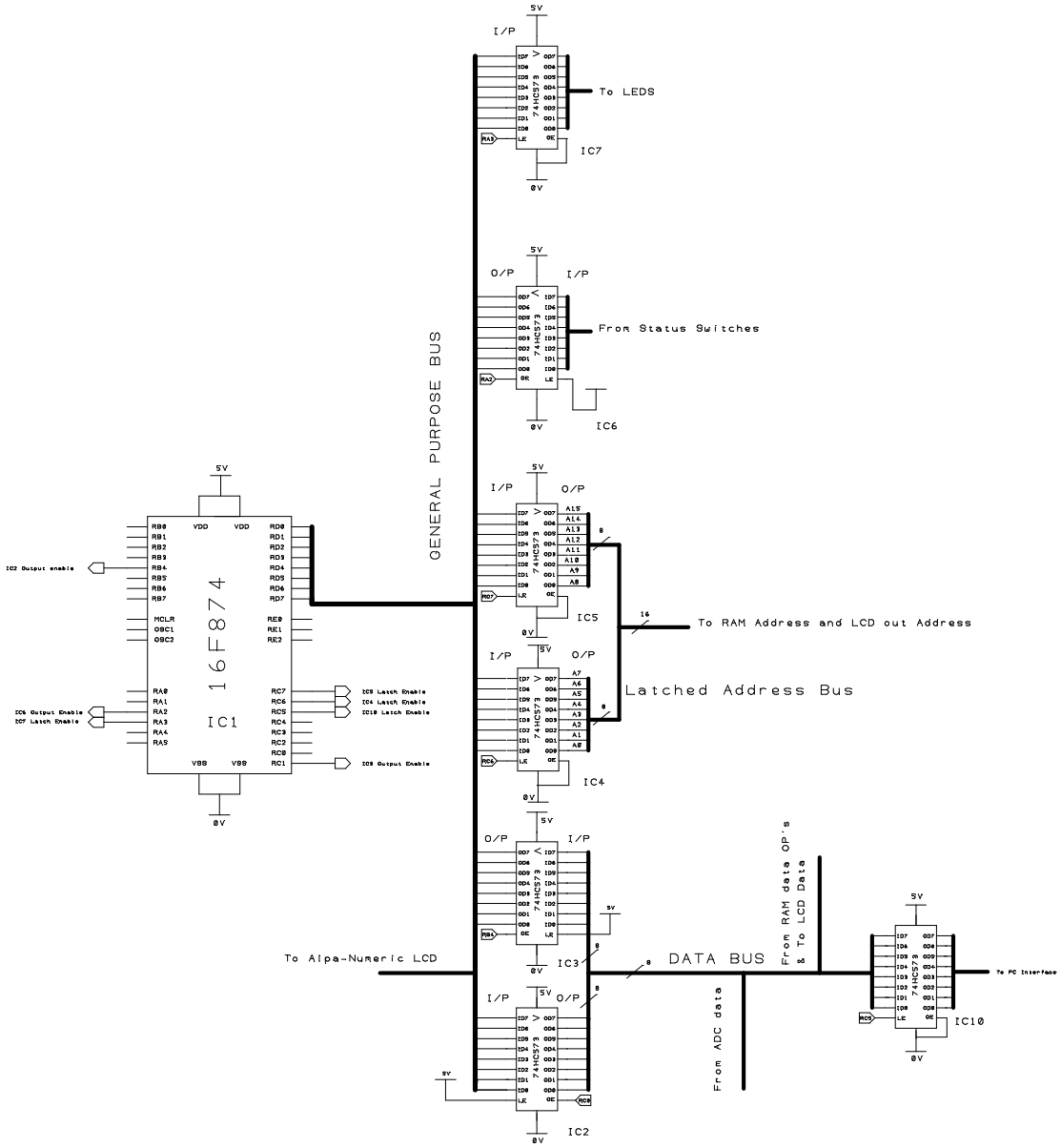

Figure 3.4.: Diagram of MCU and latch control

Data from the MCU can be sent out as outputs to the LED latch (IC7), the latched address bus latches (IC4 and IC5) and the data bus latch (IC2). Data appearing at any of these inputs can then be latched onto the outputs by clocking the appropriate latch enable pin from high to low and back again. Data will be latched onto the outputs because the output enable pin is permanently tied low. Data can be transferred onto the GPB (and in turn to PORTD of the MCU) from the data bus by setting the output enable low of IC2 and data from the status switches can be transferred to the GPB by setting the output

enable of IC6 low. It is imperative when transferring data to and from busses in this manner that the bus is freed up first as to avoid a bus collision. This could happen for example if data was transferred onto the GPB and PORTD was not set to be inputs then the outputs of both the MCU and latch would be fighting against one another possibly causing damage to one or both devices and almost certainly a loss of data etc. The data latch IC10 transfers data from the data bus to the PC data bus by setting its latch enable pin low. It can therefore be seen how latches can be very useful, in this case using 8 data bits and transferring them to different locations using only a few control lines.

The alternative approach would be to use an MCU with much more I/O pins but with the ease of use of such latches available it made sense to take advantage of them to maximise system speed and design flexibility. Indeed some latches were left unused but being there gives the system adaptability should more I/O's be required instead of remaking the PCB board.

3.3.3 Micro-Controller and random access memory control

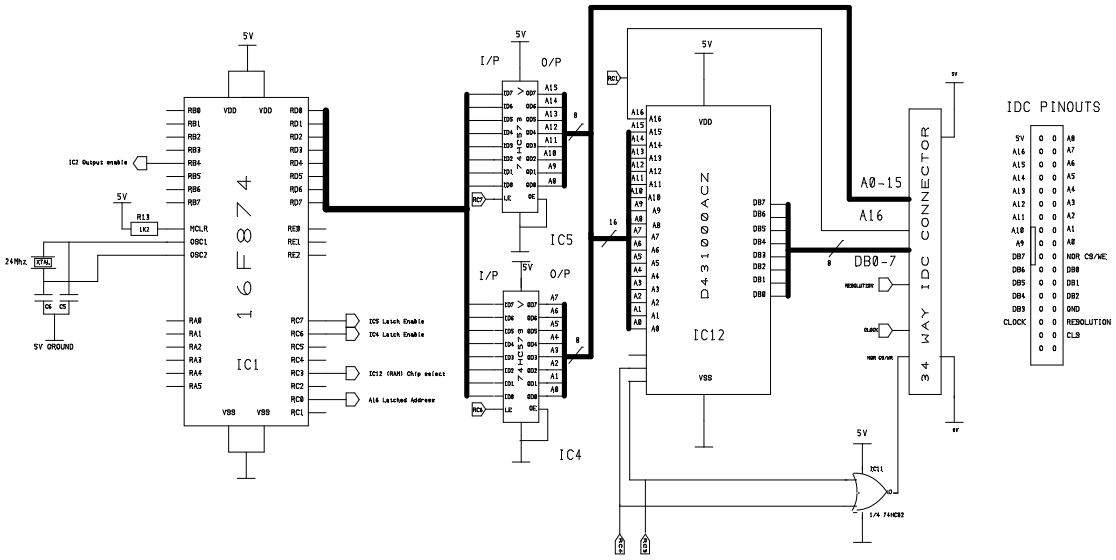

Figure 3.5.: Diagram of MCU and RAM control

The data received from the analogue to digital converter (ADC) is written into the Random Access Memory integrated circuit part no. NEC [3] (IC12), which acts as the video buffer. The RAM device

has a storage space of 128 Kbytes and hence the seventeen address lines. This stored data is then read from its particular location and appears on the data bus again ready to be transferred to the RAL system. The RAL system is completely transparent to the IADD system; it is simply a piggy-backed onto the RAL chip. The latched address also appears on the output ready to be transferred to the RAL system. The system is setup so that the data received from the ADC can be transferred onto the general purpose bus which in turn can be read and/or manipulated by the MCU. To date this functionality has not been used but was designed into the system with possible future enhancements in mind. The system has two options of sending data to the RAL system , either by an MCU generated clock or through the NOR gate which is highly efficient as the output goes high when both the RAM's chip select and its read/#write pin is low and the output goes low with all other combinations allowing for accurate timing of when data is written to RAM freeing up an extra two instruction cycles.

3.3.4 Micro-Controller and digital to analogue converter control

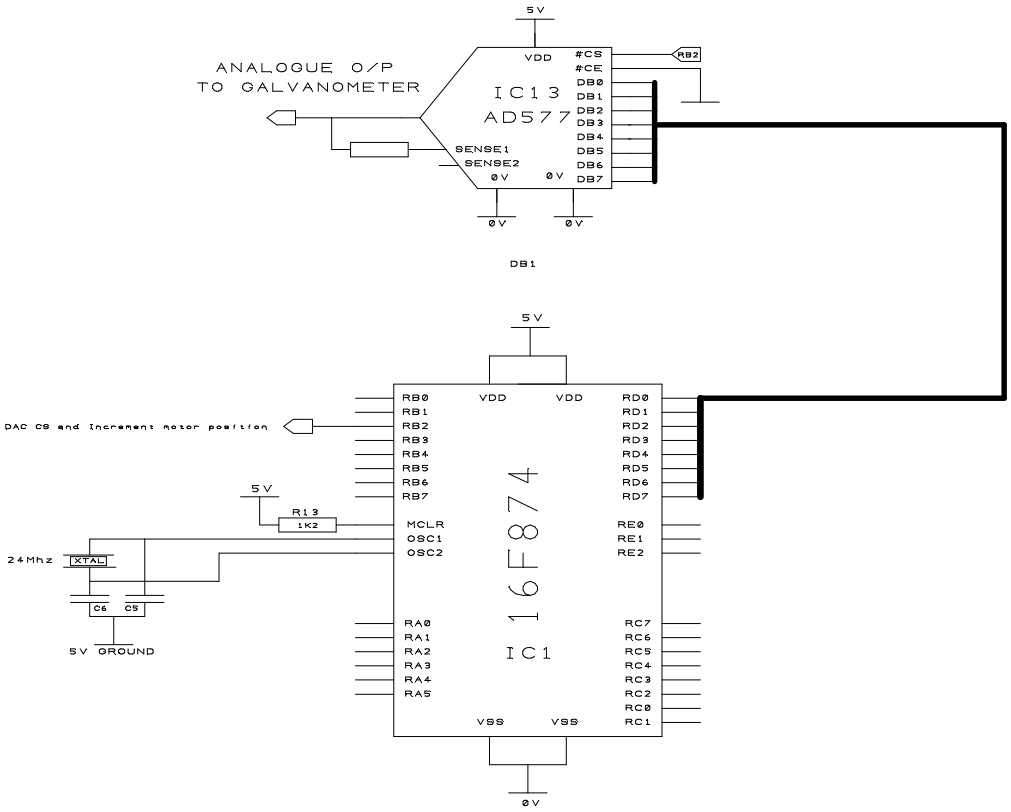

Figure 3.6.: Diagram of MCU and DAC control

The Digital to Analogue converter (DAC) used in the system is an AD577JN [4] manufactured by Analog Devices. The device was chosen for its part in the system mainly because of its simple MCU control interface, its parallel data interface, its data transfer capability along for the fact the overall ease of use due to no external components being required due to its accurate factory laser-trimmed resistor scaling. With the chip enable pin of the DAC pulled low data on the DAC output is updated when RB2 of the MCU is set low and the DAC becomes transparent therefore, no external latch is required for this device. When RB2 is set high again the data remains latched on the output of the device. For absolute maximum accuracy the DAC has two ground pins, one which is connected to the analogue ground and one which is connected to the digital ground. The IADD system has separate ground paths for this reason as with the DALC system in Chapter 2. The grounds of the DALC are connected appropriately to these separate system ground paths. Although the DAC requires no external components the output has a series resistor placed in series with the sense 1 output allowing for the output to be scaled up from the default 2.56 V to 5 V. The output of the DAC is connected to the galvanometer allowing for deflection of the Y scan.

3.3.5 Micro-Controller and analogue to digital converter control

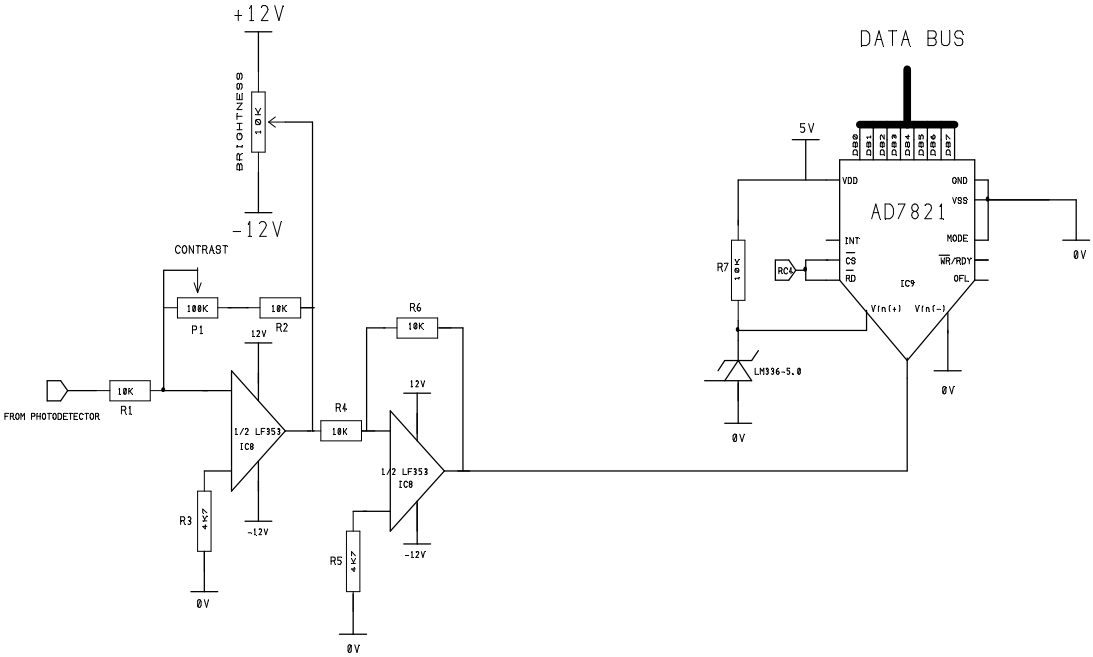

Figure 3.7.: Diagram of MCU and ADC control

The small signal from the photo-detector is amplified by the two stage amplifier and fed into the analogue to digital converter (ADC) with its data being transferable onto the data bus by MCU control. The amplifier chosen to amplify the photo-detector signal is the LF353 [5] dual operational amplifier manufactured by National Semiconductor. The high input impedance produced by the amplifiers junction field effect transistor (JFET) input stage makes it ideal for detection and amplification of the low level photo-detector output. The high bandwidth specification of the device makes it ample for the required 500 kHz maximum bandwidth. The first stage of the two stage amplifier section produces a variable gain of -1 to -10 allowing for adjustment of contrast and the second stage inverts this inverted signal back to its original phase with an offset allowing for the adjustment of brightness. The gain allows for optimum setting of the detector signal to be fed into the ADC. The ADC device is an AD7821 [6] fast sampling device manufactured by Analog Devices. It was chosen for its parallel data outputs, easy MCU interface along with its high precision (+/- 1 LSB over its full temperature range). The conversion time of 660 ns is also highly desirable. The Vin+ pin is referenced to 5 V by the LM336-5.0 [7] device which requires a pull up resistor (R7). The MCU pin RC4 controls the conversion transfer to the ADC outputs by setting the read and chip select pins low which in turn allows the data to appear on the data bus which has to be written into RAM.

The alphanumeric lcd is a 2 line x 20 character. Hitachi compatible module [8], and was included in the design to aid debugging of the firmware during its development stage. Communication is achieved to the MCU by 2 control lines and 4 data lines. (Hitachi standard 4 line communication)[9]. Port D bits 0 to 3 are connected to the high order data bit lines DB4-DB7. RS and Enable are connected to RB3 & RB6 respectively. Contrast is achieved via a 10 KΩ potentiometer is connected across 5 V and ground with the wiper being connected to the V_{adj} input on the LCD module. This allows for contrast adjust of the panel. A 200 Ω resistor is connected with the internal LED in the LCD panel. This is the backlight that allows for character viewing in transparent mode [10].

3.3.6 Micro-Controller and alpha-numeric liquid crystal display control

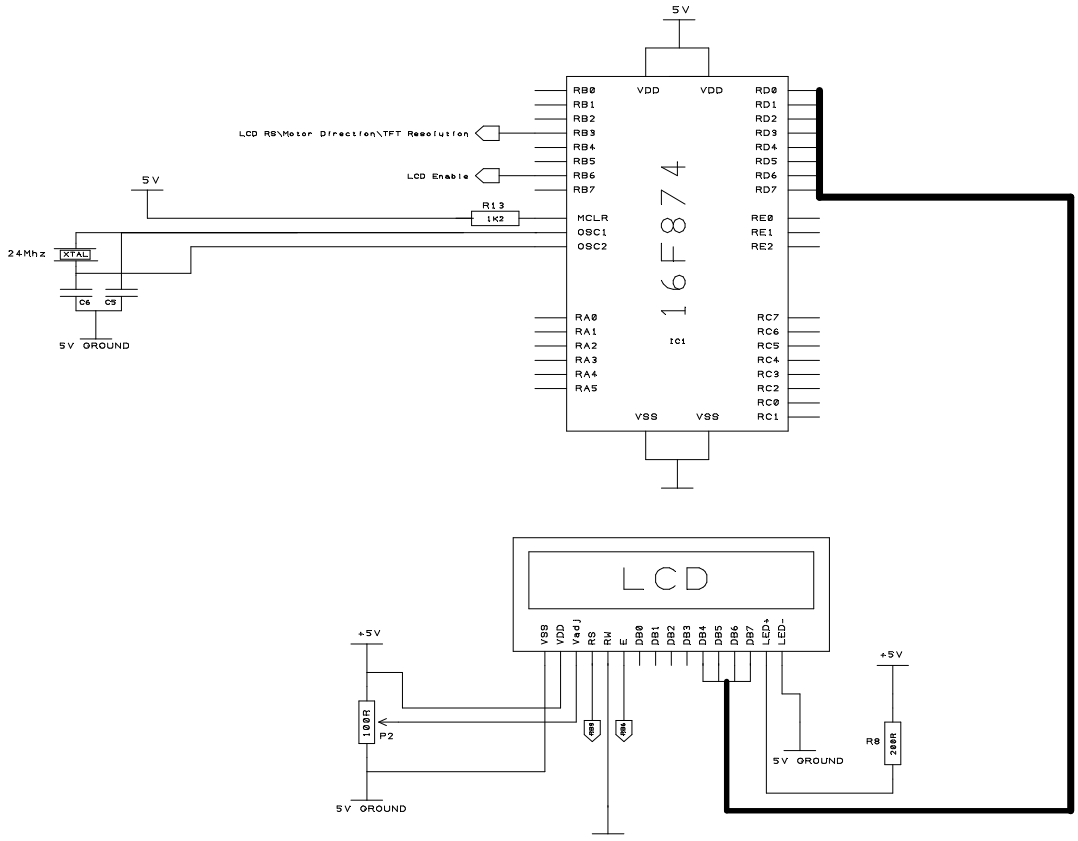

Figure 3.8.: Diagram of MCU and LCD control

3.3.7 Micro-Controller and stepper motor control

As previously mentioned a stepper motor drive option was included in the design as a potential replacement for the expensive galvanometer for use in the Y scan. The MCU has three inputs into this drive stage – half or full step, clock and clockwise or counter clockwise. The first part of the drive stage is designed around an L297 [11] motor controller integrated circuit manufactured by ST Microelectronics. The device was chosen because of its general ease of use for MCU systems with phases being worked out internally thus easing up MCU resources. The reset and enable pins are active low and are therefore tied to +5 V. The V_{ref} input varies between 0-5 V which determines the peak current able to go through the load. The control input is switched between 0 V and 5 V and when its 0

the chopper acts on INH1 and INH2 and when it is high it acts on the outputs A-D. The RC network connected to the oscillator input determines the chopper rate.

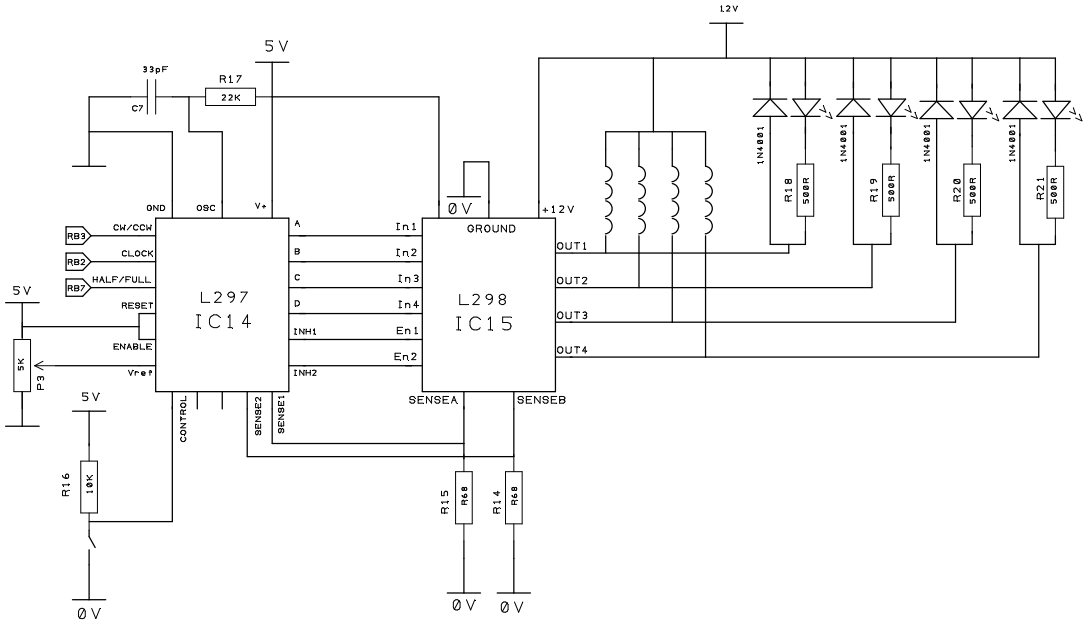

Figure 3.9.: Diagram of MCU and stepper motor control

The logic outputs of this stage are fed into an output stage built around the L298 [12] bridge controller integrated circuit manufactured by ST Microelectronics. This IC has the capability of producing the high current outputs required to drive the coils as well as being capable of handling the inductive nature of the coils. Two enable signals supplied from IC14 can disable IC15 regardless of the input signals. The two sense resistors are there to detect the current value of the load as the full load current flows down through these resistors and hence produces a voltage which is monitored by the L297 sense input pins, thus allowing for INH1 and INH2 to disable the L298 should the set current be exceeded (which is set by P3). Varying current into the coils using current feedback is called “chopping” which allows for the motor to be run with less power consumption at the expense of torque (although significantly less than simply reducing the coil voltage). The use of chopping enables high stepper motor stall speeds to be achieved with significantly less power wasted in holding current. Reversed biased diodes are connected across the coils to prevent damage to the output stage when the electromagnetic field across the motor coils collapses. Also connected to each coil are an LED and a resistor, simply to indicate when a particular coil is energised.

With this hardware stage the MCU has a very simple task of controlling the motor by use of the 3 inputs: DIR, CLK and H/F. The CLK pin advances the coil phase pattern to the next in its series in order to advance or retard the motor armature one step, the direction of which is dependant upon the logic level of DIR. The H/F input selects which coil pattern series is used; with the Full- or Half- step mode. The half step mode doubles the angular precision of the motor at the expense of torque.

We now turn our attention to the image display hardware.

3.4 Random access LCD system (RAL)

The random access LCD system (RAL) was designed for improved versatility over the DALC system in Chapter 2. The idea being that the module can be connected to any other system and used for general purpose display applications. The advanced features of the RAL system are such that any pixel of the LCD can be accessed and written to by addressing in a simple x-y-z format. It can be seen, therefore, that although primarily designed for the IADD system, any system (be it a pc or otherwise) can be easily interfaced to produce a reasonable frame rate video. The 17 bit address bus is separated into 9 horizontal bits and 8 vertical bits. This allows for graphical LCD panels of up to 320x240 to be used (¼ VGA). The core of the system, namely the dsPIC30F6014 and S1D13706 remain the same with direct interface to the Hitachi TX14D11VM1CBA TFT panel because of its excellent display properties in comparison to the Hitachi STN display (the DALC system had interface options to both Hitachi STN and TFT displays for comparison purposes). The EPROM memory used to store the introduction screen also remains on the RAL system as well as system clock speeds and configurations.

3.4.1 Components of the RAL system

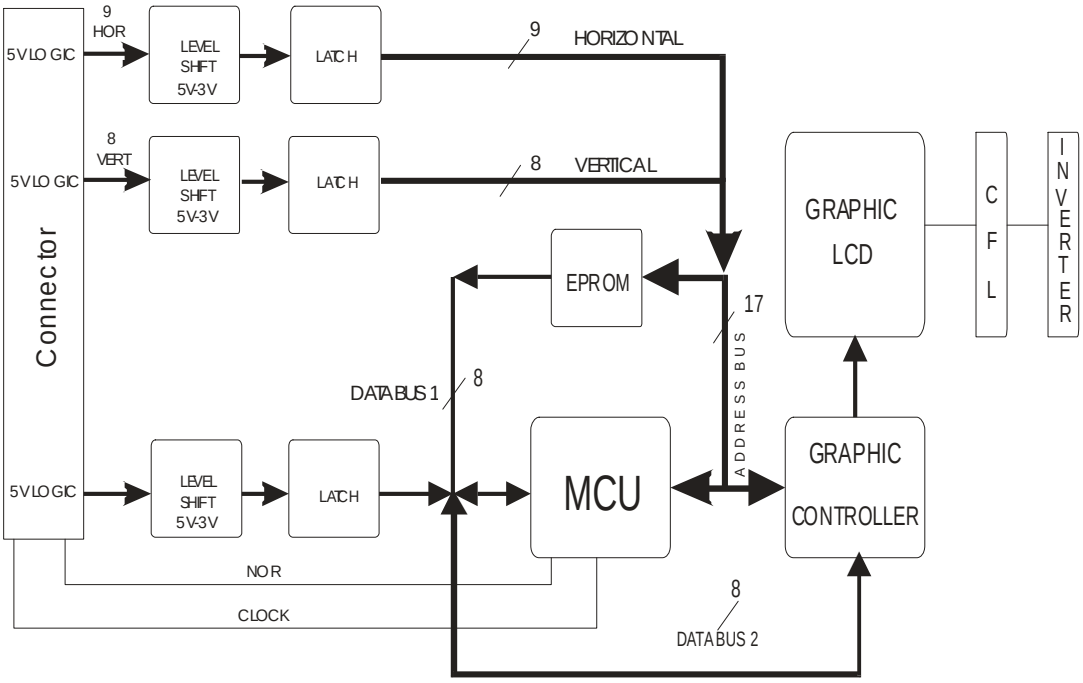

Figure 3.10.: Block diagram of RAL system

The various components which comprise the RAL system and are shown in figure 3.10 are outlined in the table below:

MCU	The MCU controls and synchronizes the whole RAL system which can be seen by the following descriptions.
EPROM	The EPROM contains a greyscale bitmap image to be displayed on the screen after switch on. It's function is two-fold: correct initialisation of the display can be ascertained and a gradient section shows the full range of allowable shades to the user.
Graphic Controller	The graphic controller reads data from its internal RAM and converts it into signals required by the LCD panel. These signals vary depending on the nature of the LCD panel being used. The controller has to be configured accordingly for different modules; this configuration being

	implemented by the MCU writing data to various registers. Most LCD panels are required to be refreshed at (approximately) 70Hz which the graphical controller handles independently thus freeing up software overheads of the MCU.
TFT Graphic LCD, CFL and Inverter.	The Graphic LCD panel produces the visual output for the RAL system. Most graphic LCD panels are transmissive meaning a panel backlight is required which is usually in the form of a cold cathode filament lamp (CCFL) with an inverter to generate the high voltage signal needed.
Level Shifting	The level shifting circuitry converts 5V down to 3.3V for use in the RAL core (due to the graphical controller utilising 3.3V supply and logic)
Data Latches	Used to transfer address data and data on to appropriate system busses and free up the driving system.

Figure 3.11: Table of RAL component functions

3.5 RAL system operation

The core of the system is the similar to that of the DALC system in Chapter 2. The following parts remain: The MCU, the graphics IC and the EPROM. The following schematic shows how they interconnect and a reminder of their operation within the system.

The MCU has a dedicated 17 bit address bus which has read/write capabilities. It can output address data to the graphics controller as well as the EPROM. It can also become set as inputs to be able to read the address of the graphics controller or indeed the address set from the IADD system. There is also a dedicated eight bit data bus which also has read write capabilities. It can write data to the graphics controller or it can receive data from the graphics controller or the data input from the IADD system. This is a slightly different design compared to the DALC system which had two data busses, one which connected to the graphics controller and one which interconnected the rest of the data.

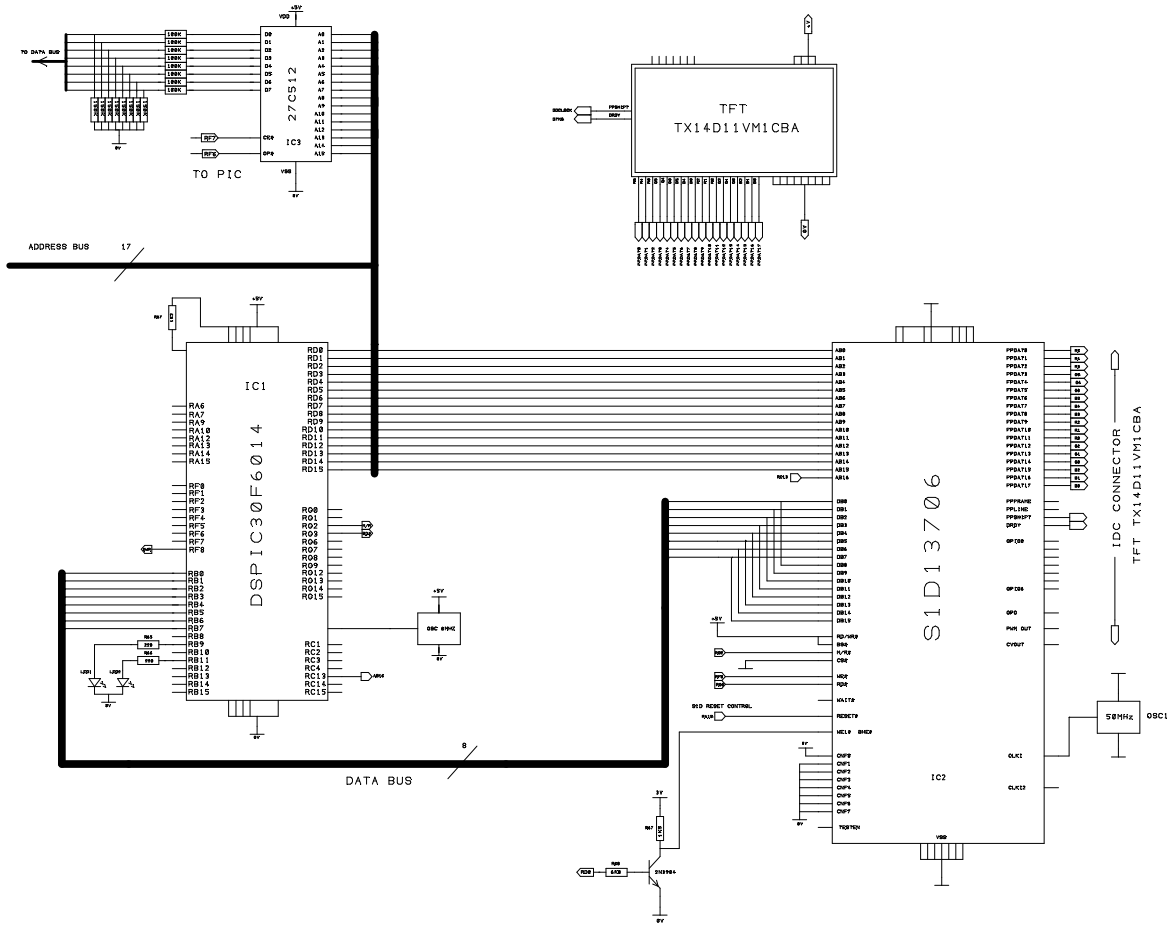

Figure 3.12: Diagram of RAL system core

The MCU runs from a 7 MHz clock which is multiplied by an internal PLL by a factor of 16 to give an MCU clock input of 112 MHz. The instruction cycle is therefore 35 ns. The other I/O pins of this system core are the basic control pins between the MCU and EPROM and the MCU and graphics controller as described with the DALC system. The EPROM as in the DALC system is used for storing data for an introduction screen at switch on. All the other hardware and configuration settings are the same as the DALC system. The MCU software runs in a different manner to that of the DALC system which will be described later. Two status LED's are implemented into the design as opposed to four in the DALC system.

The interface from the IADD system to the system core is shown in figure 3.14

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3.5.1 RAL and DALC system differences

This is where the RAL system differs greatly from the DALC system with improved architecture implemented for greater performance. The key to this is the design of the IADD system allowing for easier faster access to any memory location and hence, any pixel of choice. The key advantage of the RAL system is that it is completely transparent to the IADD system whereas the DALC system required two way communication with the external data acquisition system for each pixel. The downside is that the RAL system has to be fast enough for incoming data otherwise it will miss data reads. This is achieved by writing streamlined software taking advantage of the dsPIC's architecture.

The data for display is presented to the 34-pin IDC connector, and is separated into three components: address, data and handshaking. The address is subdivided into 9-bits of x-data and 8-bits of y-data (i.e. sufficient to address any pixel over the 320x240 area of the display module. The pixel intensity data is presented at a resolution of 8-bits and with 64 shades of grey being displayed the lookup table was formatted as follows. Location 0-3 of the lookup table were allocated shade 0 (so if data value 0,1,2 or 3 were written to the Epson IC then shade 0 i.e. black, would be displayed). Locations 3-7 would have shade 1 and so on. This is how the 256 shades displayed on the PC are divided down for the maximum allowable 64 shades that the LCD panel can display.

Handshaking takes place on a single line, clock, on whose falling edge the address and data lines are latched into their respective busses ready for processing. The data was latched in this way in order to reduce the requirement of the external driving system (in this case, the IADD) for keeping the address and data valid for an undue period of time. The option of an additional handshaking line is available but not used in this system called the 'busy' line. This is available if required for other systems which may download data quicker than the current IADD system to the RAL than the 10 frames per second maximum frame rate. A reminder of how this 10 frames per second specification is required is as follows. With the OPO laser system firing at a maximum frequency of 350 kHz the throughput of the RAL would expected to be capable of pixel execution and display speeds to match these frequencies. The chosen resolution modes for the system are low resolution 160 x 120 pixels and high resolution 320 x 240. Whatever the frame resolution mode is set up for i.e. 160 x 120 pixels (19200 pixels per

frame) or 320 x 240 (76800) pixels per frame, dictates the maximum display frame rate of the system. For example, if the mode is set up for 160 x 120 pixel resolution the maximum frame rate would be 350 kHz/19.2 kHz which would equal 18.23 frames per second. If it was set up for 320 x 240 resolution the frame rate would be 3.18 frames per second. However, as in Chapter 2, due to limitations in the scanning hardware the maximum possible frequency obtainable is 120 kHz giving frame rates of 6.25 frames per second (low resolution) or 1.56 frames per second (high resolution). Again with this in mind the throughput of the RAL system was designed for slightly higher frame rate capability than required which was roughly equal to 10 frames per second at low resolution or roughly 2 frames per second at high resolution. To achieve these results on the falling edge of each clock input to the RAL system the data and address values must be encoded and written to the buffer memory of the Epson graphics controller in less than 6.6 μS. ($Tpixel = \frac{1}{150kHz}$). Section 3.5.2 shows that the period of pixel execution is 6.2 μS and thus achieving the specification of 10 frames per second. If the scanning system or any other system processed data quicker than the RAL system the busy line would be held in a state indicating to the host system that it is not ready to receive more data and the host system would stay in a wait state until the busy status changes. The firmware for the MCU was written in assembly language to maximise speed and code efficiency, although a more recent evolution of the RAL, featuring a faster processor with better streamlined code, has now been realised which uses firmware written with mixed C and assembly (see chapter 5).

As in the previous chapter, the code listing will not be presented here for the sake of brevity but appears in the appendix and on the included CD-ROM. The code is split up into three sections: dsPIC initialisation and EPSON driver chip setup, display of the onboard background image (as stored on the EPROM) and display of the code presented at the external connector. Clearly, the first two of these segments is executed once at start up. The dsPIC port setup routine simply defines the direction of each pin / port. The handshaking lines between the external connector, EPROM and EPSON chips are all outputs and remain so throughout the code execution, whereas the address bus direction changes once the code is in the repeating loop which displays the data clocked in from the external connector. This is required as the data incoming is in cartesian (x-y) address format, whereas the EPSON is addressed sequentially from 0 to 76799 (i.e. 320x240 pixels). Due to the finite number of pins, the x-y format address data is clocked in on the address bus, the sequential address calculated and then the address bus

direction is changed (after making the address latches tri-state) before sending the address data (now in sequential format) to the EPSON.

The EPSON setup routine defines the type of LCD module attached to the device (i.e STN, TFT, resolution, etc) and, importantly, the colour look up table. As in the previous chapter, the same values are written the red, green and blue channels in order to produce a grey-scale image.

Once the dsPIC and EPSON have been initialised, image information is ready to be written to the screen. Before polling the external connector, the image stored on the EPROM is displayed. This currently has a graduate-scale upon it to indicate to the user the available dynamic range of the display module and, at the development stage, allows the programmer to see that the display module has been correctly initialised.

Lastly, an infinite loop is entered which begins with both the latches being both transparent and their output low impedence before the polling of the CLOCK pin. Upon its falling edge, the latch enable pins on each latch falls to clock valid data into the board. The use of a fast microcontroller and streamlined assembly language programming results in the address and display data being latched onto the bus as quickly as possible after the falling edge of the external clock signal, and this defines the requirement for the external system (i.e. IADD) to keep valid data on the bus for as little time as necessary after the falling edge of CLOCK. As outlined above, the address data is read into the microcontroller where it is converted from cartesian to sequential address data, using the simple equation ADDR=(320*Y_ADDR)+X_ADDR. Here the use of an advanced microcontroller with a dsp capability is beneficial as the chip has an integrated multiplication module which allows the multiplication of two 16-bit numbers to give a 17-bit result in a single clock cycle. Previous devices in the product range would have required a multiplication algorithm programmed in firmware, with obvious time penalties. The display data is not acquired into the dsPIC as it is bussed directly from its latch into the EPSON display driver. Once the sequential address has been placed on the bus, the address and display data are clocked into the EPSON, ready for display.

The two key timing parameters of the module are, then, the time taken to latch the address and display data onto the card after the falling edge of CLOCK, defining the requirement of the external drive logic to keep valid data on its output bus, and the time required to process the address data from cartesian to sequential data and clock it, along with the display data, into the EPSON display driver, thus defining the maximum rate at which data can be written to the module. It is highly desirable to minimise these two parameters, and their actual values will be discussed in the results section below. Figure 3.13 shows a diagram of how easily the RAL system can be addressed and written to.

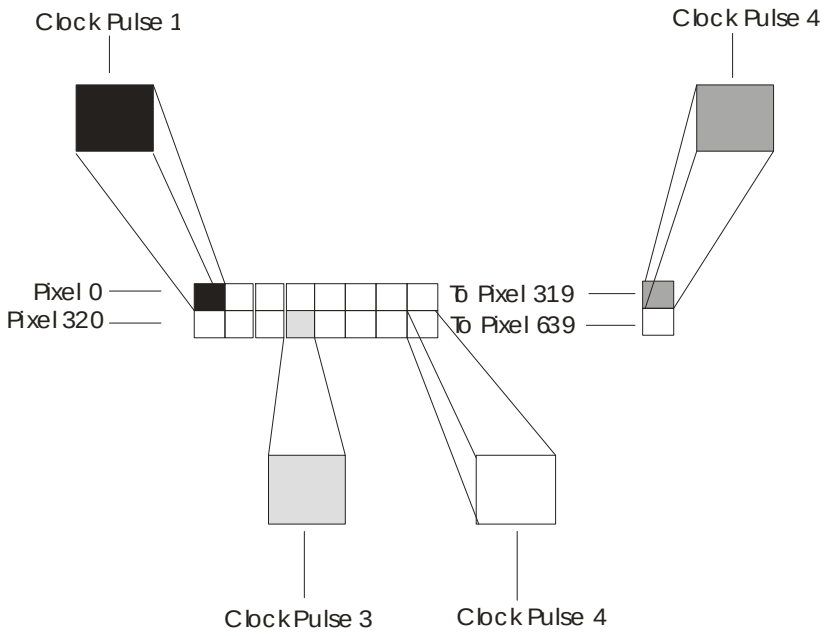

Figure 3.13: Diagram of simplistic addressing/writing modes of the RAL system

On the falling edge of clock pulse 1 the address is A0-9=0 and A10-17=0 giving an encoded address of 0 being written to the Epson graphic IC's buffer memory. The data value on the D0-7 inputs is 0 which is passed onto the lookup table of the Epson IC. The result is pixel 0 on the LCD panel is black. On the falling edge of clock pulse 2 the address is A0-9=7 and A10-17=1 giving an encoded address X value of 7 and a Y value of 1. The data at the systems input is 255 and hence displaying this pixel as white.

On the falling edge of clock pulse 3 the encoded address is X=3 and Y=1 with a data value of 180 making this pixel display a lighter shade of grey. Finally, on the falling edge of clock pulse 4 the encoded address is X=319 and Y=0 with a data value of 100 making this pixel a darker shade of grey. It can be seen how easily a greyscale image can be constructed and displayed on the RAL system.

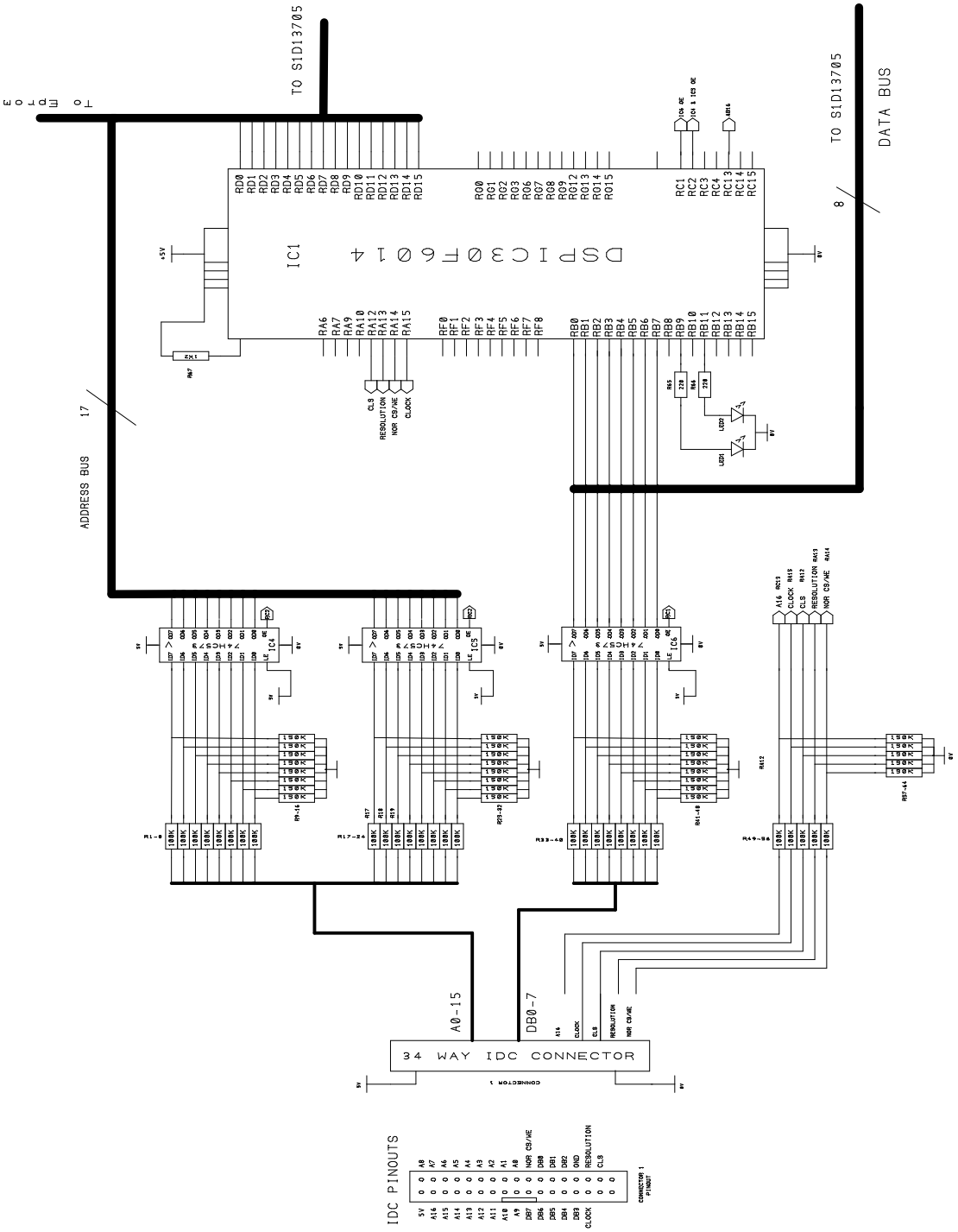

Figure 3.14: Schematic diagram of RAL system

3.6 Chapter 3 Results

We will separate the results gained over the course of this work into three subsections, namely the performance of the stepper motor mirror drive, that of the IADD and finally the LCD display module.

3.6.1 Stepper motor.

As outlined above, the electromechanical scanner requires a reciprocating mirror in order to facilitate the y-scan of the illuminating beam. This was initially achieved through the use of a galvanometer and whilst its performance was excellent, the very high cost of this component makes a cheaper alternative highly desirable. Hence a stepper motor was evaluated in this context. The y-scan required 100 lines to be scanned over ~±12°, giving a required mirror rotation of only 6° in between successive area (i.e. 0.06°). As it is not possible to purchase a stepper motor with such a fine step angle, we utilised a geared pulley system in order to improve the angular resolution, as shown in figure 3.15a. Here, a standard high precision motor exhibiting 200 steps/revolution (1.8°/step) was coupled to the mirror armature via two geared sprockets and toothed belts, giving the required mirror step size of 0.06°. In between each armature a tensioning pulley was included to reduce the effects of back-lash in the system as the direction of scan was reversed. Such an effect would introduce a loss of registration between successive upward- and downward- scanned images. Figure 3.15b shows a photograph of the more expensive galvanometer.

The stepper motor assembly was integrated into the scanning head and interfaced to the IADD. Of crucial importance to the required frame rate of 10 frames per second was the maximum frequency at which the motor could be pulsed. Clearly, bandwidths in excess of 1 kHz are required in order to achieve 8 f.p.s.

When the motor was operated without load (i.e. when disconnected from its geared assembly) we found that it operated up to a stall speed of 2.35 kHz, leaving a comfortable margin over the required

1kHz. This was in the absence of current chopping and mean current drawn was 3.2 A. Once this was introduced in order to reduce current load on the IADD the stall speed was reduced to 1.8 kHz with a mean current draw of 1.3 A, thereby yielding a >50 % drop in current requirements with a significant, yet modest drop in performance.

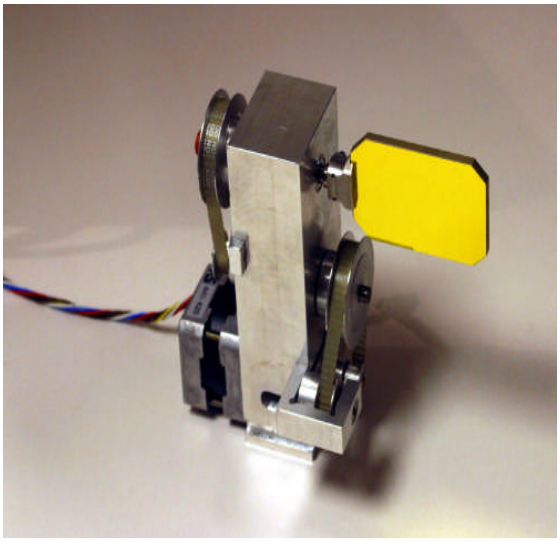

Figure 3.15a: Photograph of the stepper and motor and drive system.

Figure 3.15b: Photograph of the galvanometer

Once integrated within the mechanical geared sprocket system, necessary to achieve the required angular resolution in mirror deflection for y-scan, extra load is placed on the armature of the stepper motor, yet further reducing the stall speed. The assembly was integrated into the polygonal scanning

system and images acquired. Initial scans showed excellent performance in terms of single frame acquisition where mirror deflection occurs in a single direction (i.e. mirror moving either up or down) scans, but registration between successive frames was out of synchronisation due to the gearbox backlash although some effort was put in to minimise this as mentioned above.. The mechanical design could be improved to compensate for this but it was decided this would play no further part in the context of this research programme.

3.6.2 Performance of the IADD system

The performance of the IADD system was generally good, the main advantage over the acquisition electronics previously designed in house which subsequently drove the DALC system is one of flexibility and interface simplicity. The flexibility to drive and evaluate the performance of the stepper motor and indeed the galvanometer was of huge advantage. With the performance of the stepper motor being mixed this allowed the research to continue with the overall better performing galvanometer albeit significantly more expensive. The interface simplicity and communications protocol designed to drive the RAL system proved a much better idea than the original interface. Perhaps the IADD system could have been improved with low noise techniques similar to that in Chapter 2 to improve overall image quality. However, with the core design now present future implementation of such techniques could easily be implemented. Figure 3.16 shows a picture of the IADD board.

3.6.3 Performance of the RAL system

The performance of the RAL system proved a real success. The random access ability to address and subsequently write to any pixel makes this part of the system a very useful part of the overall project and indeed could be implemented seamlessly into other systems due to the modified and simplistic x-y address format. The RAL system specifications of 6 frames per second were reached. The choice to maintain the core components form the DALC system in chapter 2 proved to be the correct decision in terms of design time and excellent performance. A photo of the RAL system is shown in figure 3.17.

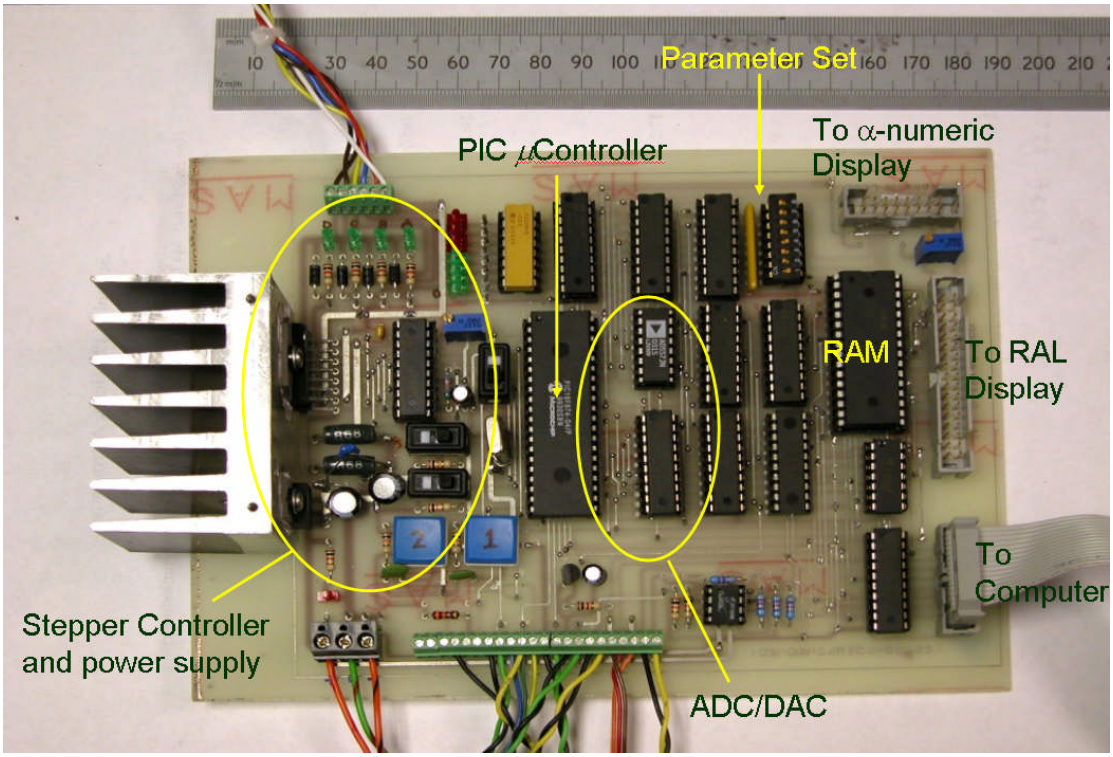

Figure 3.16: Picture of the IADD board.

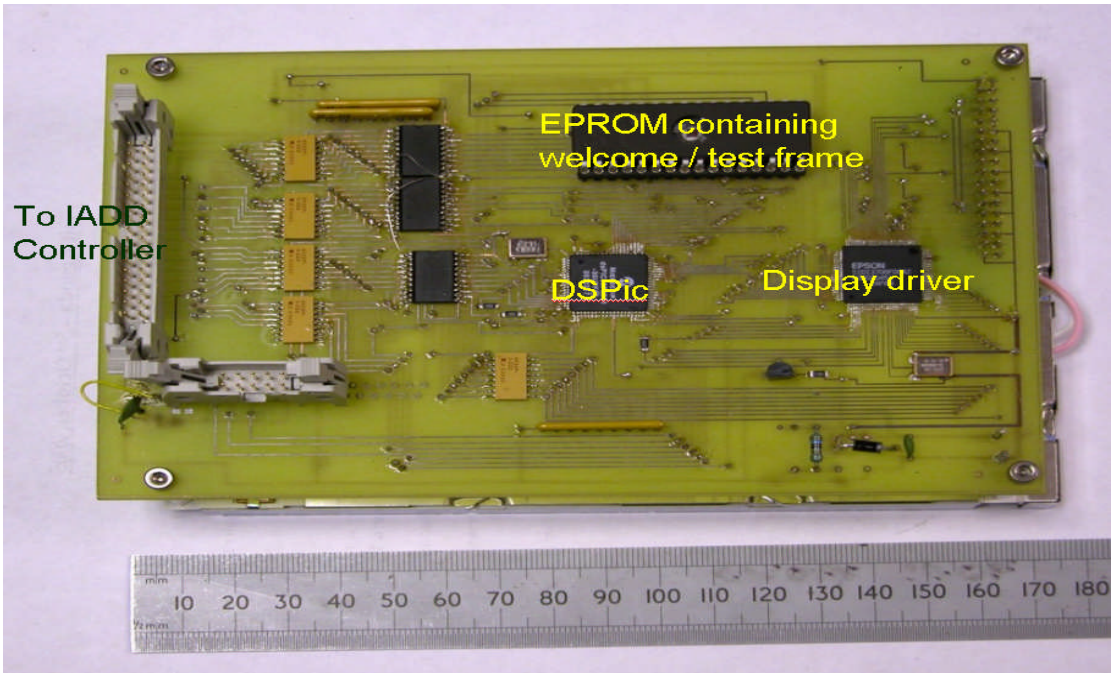

Figure 3.17: Picture of the RAL system

Figure 3.17 shows the real life photograph of the methane being ‘leaked’.

Figure 3.18 show the complete Hyperspectral Imaging System imaging methane from a gas tank.

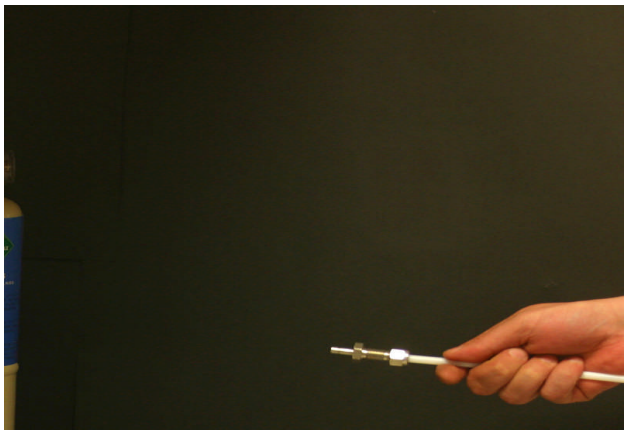

Figure 3.17:Photograph of the invisible methane “leak”against a dark backgound

Figure 3.18: Picture of the Hyperspectral Imaging System

3.7 Summary

The research in this chapter proved very fruitful indeed. With the notable introduction of the modular approach the success of the RAL system is significant. The standalone module surpasses it's requirements in terms of frame rate execution and its easy interface makes it a possibility in other imaging applications. With an introduction of a slightly newer pin for pin compatible MCU appearing on the market towards the end of the research in this chapter, implementing this into the design along with possible streamlining of code could allow for frame rates to reach a possible 15 frames per second at full 320x240 resolution. Although this is far greater than required for this research it certainly makes it a possible attraction for other system requiring frame rates of these quantities. Another possible improvement could be the removal of the current CCFL backlit TFT display and replacing it with an LED backlit version. The reason for using the CCFL version initially was one of cost and availability. When the research programme first started LED backlit versions were rare and very expensive however due to the fast developing world of electronics and price crunching of in-demand products these versions are readily available at comparable prices. The introduction of a backlit TFT screen would eliminate the need for the bulky inverter used to drive the florescent lamp and also eliminate the need for high voltage in the system and thus reducing the possibility of injecting other parts of the system with noise.

The IADD system could do with improvements such as the introduction of low noise techniques to allow for higher quality imaging, however, the fundamental operation of the system proved excellent, acquiring data and delivering it to a PC or the RAL system or indeed both simultaneously. The inclusion of the stepper motor circuit on the IADD board allowed for research into replacing the galvanometer with a stepper motor and thus reducing system costs significantly. However, it was proved that the galvanometer had better performance although time could be invested the mechanical design of the stepper motor drive system could possibly yield performances to that of the galvanometer.

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Chapter Four – Laser Management System (LMS)

4.1 Introduction

With the electro-mechanical scanner control module and image display electronics completed, we now turn our attention to the final part of this research programme, namely the control system for the laser illumination source which is at the heart of this hyperspectral imaging system. This, the 'Laser Management System' (LMS) was left until last in the research programme as it was already possible to operate the OPO with commercially available electronic drivers and diagnostic instrumentation in a way which was not possible for the scanning head and display.

As will be outlined later in this chapter, the requirement for the LMS is to provide dual channel temperature control for the pump laser diode and nonlinear crystal, a constant current supply for the pump diode and support electronics for the pre-purchased RF accousto-optic Q-switch driver [1]. Whilst it is highly desirable for this instrument to be battery operable, we chose not to implement full battery support at this stage in development (i.e integrated lead-acid battery and associated charge controller electronics) but did design the system to operate from a single rail 12 V supply in order that the laser could be operated and evaluated remote from the research laboratory if necessary.

Before a detailed discussion of the LMS design, we will briefly recap the physical mechanism underpinning the tuning mechanism employed in the laser system.

4.2 The parametric process, quasi phase-matching and temperature tuning

The parametric process works by dividing the energy of a high energy pump photon between two lower energy generated photons, designated the 'signal' and 'idler'. By convention, the lower energy (i.e. longer wavelength) generated photon is designated as the idler. In the system outlined in this report, it

is the longer wavelength idler photon which is extracted as useful output. From conservation of energy, we have:

$$\nu_p = \nu_s + \nu_i$$

Where ν refers to frequency and the subscripts *p*, *s* and *i* refer to the pump, signal and idler respectively. This equation indicates that the frequencies of the two generated waves add up to the frequency of the pump wave, or in other words the sum of the energies of the signal and idler waves is that of the pump wave. From this equation it is clear that there are an infinite combination signal and idler frequencies that could add up to the pump frequency. Whilst the parametric process is indeed a broadly tuneable one, the device does not produce such a broad range of wavelengths simultaneously. This is because, in addition to the conservation of energy condition mentioned above, there is also the requirement of conservation of momentum, or *phase-matching*.

Phase-matching means that the three waves present within the nonlinear crystal (i.e. the pump, signal and idler) all maintain the same speed (and therefore phase) whilst propagating through the nonlinear crystal. If they do not maintain this condition then the energy transfer process becomes very inefficient, and can even work in reverse whereby energy flows from the generated signal and idler waves back into the pump wave. The speed of light in any medium is a function of the mediums' refractive index, *n*. Unfortunately though, *n* is also a function of wavelength (hence the rainbow effect observed in dispersive components such as prisms). Hence, in a 'normal' optical material such as glass, phase-matching of the pump, signal and idler is not possible as the three different waves experience a different refractive index and therefore travel at different speeds. Special techniques have to be employed in order to meet the phase-matched requirement in the non-linear crystal utilised in the laser system.

A detailed discussion of these techniques is beyond the scope of this research programme and report, but will briefly be mentioned here for the sake of completeness. Early non-linear devices used bi-refringent non-linear crystals whose refractive index was a function of crystal angle. Hence, the same wavelength propagating at different angles within such a crystal experienced a different refractive

index. It was soon realised that this phenomena could be used such that different wavelengths experienced the same refractive index – and hence propagated within the crystal at the same speed (i.e.with the same phase). Thus, the phase matching condition was met. The disadvantage with this scheme, though, was that experiments were limited by the crystals they had available to them, which did not have the right birefringence to allow then to phase match for any arbitrary wavelength.

In the late 1980's, periodically-poled (or quasi-phase matched [2]) crystals became available. In these crystals, special 'domains' were written into the crystal to keep the different wavelengths in phase. This works by letting the wavelengths slowly drift out of phase as they would in any bulk solid, but then 'reset' the phase at a domain wall. As the domain size (or *period*) could be chosen arbitrarily, the phase matching condition could be met for any wavelengths within the transparency range of the crystal.

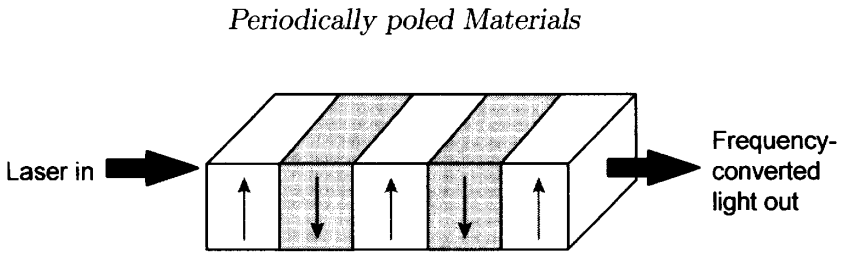

Figure 4.1: Periodically poled material. The sign of the non-linear coefficient is 'flipped' every period to correct for phase miss-match [2]

Now, the particular signal and idler wavelengths that meet the phase matching condition are the ones which will be generated by the parametric process. The phase matching process is still heavily dependent upon the refractive index of the crystal and crucially, in the context of tuning the system, the refractive index is dependent upon temperature. Therefore, *the wavelengths of the signal and idler fields can be tuned by varying the temperate of the nonlinear crystal.*

The relationship between the wavelengths present in the system and the refractive index then experience within the nonlinear crystal is given by

$$\frac{n_p}{\lambda_p} = \frac{n_s}{\lambda_s} + \frac{n_i}{\lambda_i}$$

Here, n_p, n_s and n_i are all dependant upon temperature. Hence, we can see that the wavelengths generated by the parametric process can by tuned simply by changing the temperature of the nonlinear crystal.

Figure 4.2 shows how the signal and idler wavelength tune as the temperature of the crystal is varied. In this system, the grating period written into the quasi-phase matched nonlinear crystal has been chosen such that the process phase matches for the desired methane absorption wavelength slightly above room temperature in order to allow for easy temperature stabilisation. We can see that the idler wavelength matches that of the peak absorption in methane (3.31μm) when the nonlinear crystal is at a temperature of ~41.5 C.

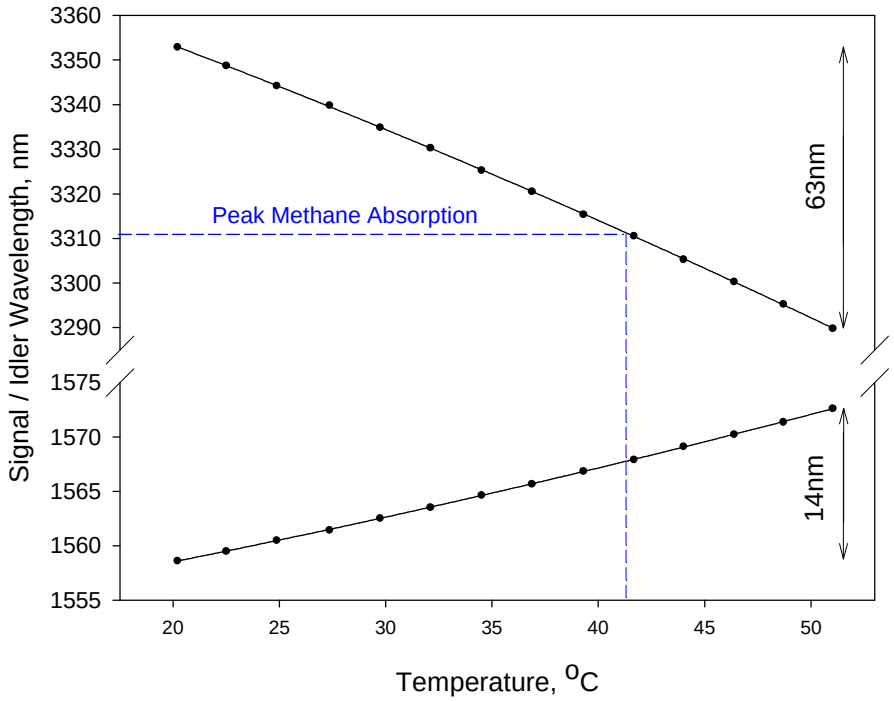

Fig. 4.2.: Temperature tuning of the signal and idler waves

These curves can be predicted by using the so-called Sellmeir equations, but these are too complex to implement by the simple embedded processor which will be utilised in this system. By fitting a simple

quadratic equation of the form $\lambda=aT^2+bT+C$ to the experimentally measured results, we can relate the idler wavelength to the crystal temperature with a very simple programmed algorithm, and vice-versa. This equation, with it's fitting parameters is then programmed into the temperature controller processor in order for the user to be able to set the wavelength of the laser system directly. We can see from this figure that around the desired operating point, the idler tunes at approximately 182 GHz/°C. Given that the methane absorption feature we are tuning to exhibits a bandwidth of ~20 GHz [3], a temperature stability requirement of ~100mK is placed upon the temperature control system.

It is necessary to control the temperature of the pump laser diode within the laser system as its output wavelength needs to closely match into the peak absorption manifold of the laser gain medium which it is pumping. This absorption feature is reasonably wide approx 450 GHz [4] and so the requirement for servo loop accuracy and stability is somewhat reduced in comparison for that of the nonlinear crystal, given that the laser diode tunes at approximately 0.3 nm/°C (138 GHz/°C). This results in a required temperature stability of ~±1°C However, in order to maximise the optical output power stability of the OPO the pump diode temperature (hence wavelength) will be stabilised to the best stability offered by the servo design implemented.

A Q-switch is integrated into the system in order to produce a rapid train of optical pulses; one fired off for each pixel measurement. Whilst the low-threshold properties of the intracavity OPO technique make the possibility of operating the device in the continuous-wave regime a possibility, the inclusion of the parametric effect within the cavity leads to unpredictable and long lived amplitude oscillations of the pump, signal and idler fields [5]. The laser is therefore Q switched at a high repetition rate to eliminate these oscillations. An oscillator and monostable timer is therefore required in the LMS in order to generate the Q-switch driver control signal of the correct frequency and duty cycle. The monostable timer can either be triggered by the internal oscillator for stand alone laser operation, or externally by the image acquisition system in order to synchronise the firing of the illuminating laser pulse and the acquisition of the detected backscattered light.

4.3 Laser Management System.

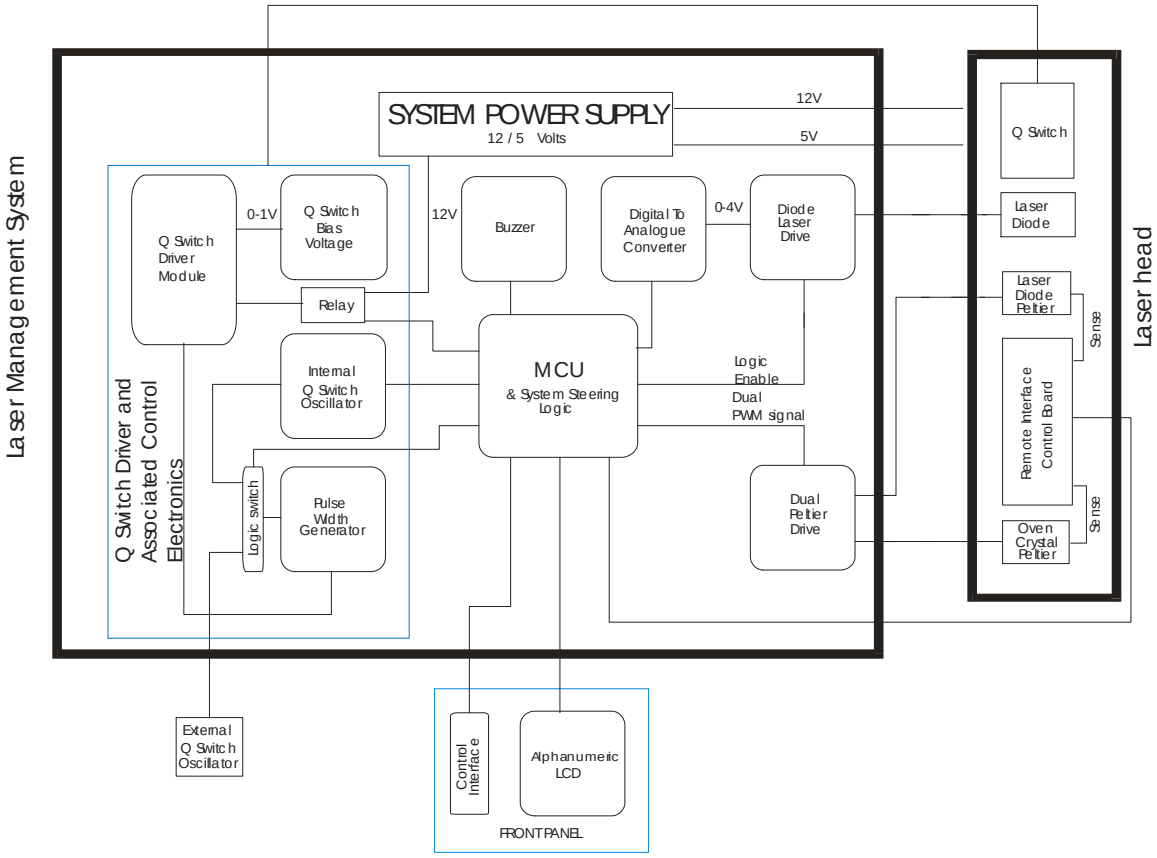

Figure 4.3. : Block diagram of Laser Management System

The LMS system could be designed mainly with analogue electronics using temperature controller modules for temperature control, however, going down the digital route allows for much a better human controlled interface along with very cheap components in comparison. With these facts in mind it was decided that the temperature control design would be implemented with a digital core.The four electro-optic components in the laser module, namely the laser diode, Q-Switch, laser diode TEC and nonlinear crystal TEC are all controlled by the Laser Management System (LMS). The operational

parameters of these components are set by the user and stored in non-volatile memory within the laser head ready such that they can be recalled by the LMS when switched on. In this way, any particular head (assuming a future production run) could be used with any LMS without the need to reprogram these parameters.

The user selects parameters such as laser diode current and operation wavelength (via nonlinear optical crystal temperature) from the front control panel of the LMS. This is done via three push buttons, a key switch, a rotary optical encoder (for user input of scalar values) and an alphanumeric LCD display. In order to simplify the front panel, parameters are entered via various menus which are selected via the front control panel 'menu' button. The menu switch allows for rotating through various menus and whilst on the particular menu in question pressing the edit switch allows for parameter values to be changed by the rotary encoder. Two additional switches are implemented into the system, a key switch which allows for laser diode operation to be enabled (in accordance with accepted safety practices) and one push button switch which toggles the laser diode on and off. The buzzer is the final part of the human I/O interface which gives audio feedback in certain situations.

A "factory setup" menu is also available for setting values specific to a particular laser system which, once set, would not normally need to be modified except in the case of component replacement. Such parameters include two sets of proportional, integral and differential parameters for the laser diode and nonlinear crystal PID loop (allowing for precise temperature control of these two components), the idler wavelength a, b,and c polynomial curve fitting parameters and the laser diode maximum current. Tweaking these former parameters gives different temperature responses over time. These form the PID parameters in the algorithms used for temperature control. The algorithm result is processed by the MCU and this value is delivered to the TEC drive output stage which sets the correct power in the TEC allowing for accurate temperature control of the laser diode and the nonlinear crystal oven. The accuracy and stability of the temperature response depends on the correct tuning of the PID parameters which will be discussed further in section 4.5.4.

A brief description of the parameters which can be set in normal operation are as follows. The laser diode has two parameters which can be set, namely the laser diode current (3.2 A max) and an on/off

which is controlled by a switch on the front panel. The settings for the associated electronics for the Q switch driver that can be varied are a Q switch enable/disable, the system can be selected for either an internal or external oscillator and a bias voltage for the driver. In addition to this the frequency and pulse width of the internal oscillator can be adjusted. The internal clock signal for the Q-switch driver (repetition rate, duty cycle) are set by trimmers within the LMS and are not accessible from the front panel menu screens.

This section gives a brief description of the various system parts and how they operate and combine to control the laser head, with reference to figure 4.3. A more in depth technical explanation follows in the next section.

4.4 Brief description of LMS components.

The following table outlines the key components of the LMS and their function.

MCU and Support Logic	The MCU is the heart of the system and controls the various parts with direct or indirect interface. The support logic aids the MCU with dedicated tasks to help carry out particular operations i.e. PID temperature control.
Dual TEC Drive	The dual TEC drive circuit supplies the high current bipolar output drive required by the TEC's to be able to control their individual loads (the laser diode and the oven crystal). This stage is controlled by the MCU and system support logic by means of PWM control. .
Laser Diode Drive	The laser diode drive circuit supplies the low noise laser diode output current. This stage is controlled by the MCU (via a DAC) and the support logic.

Remote Interface Control Board (RICB)	The RICB is located in the laser head and has the responsibility of obtaining the current temperature of the laser diode and oven crystal temperature and feeding this data back to the MCU to allow the MCU to process the data and control the temperature as required in the form of a PID software loop. In order to minimise the effects of noise, the temperature of the laser diode and nonlinear crystal are sampled and digitised by the RICB before transmission to the host LMS. This board also has EEPROM memory to store the system parameters specific to the laser system in which it is installed, and added safety features to protect the laser diode from the effects of static discharge. The MCU controls the data feedback, the memory read and write along with the added safety features.
Q Switch Drive And Associated Control Electronics	Control Electronics combine to control the driver unit with the option of an internal/external drive oscillator. The MCU and system steering logic has control over the associated control electronics with the exception of the pulse width generator and the Q switch Bias voltage.
System Power Supply	The system power supply produces power for all the electronic sub-systems within the instrument which run from 12V DC and 5V DC.

4.5 Electronic System Design

The microcontroller unit used in the LMS system is the PIC18F452 manufactured by Microchip Technology [6]. The device is an 8 bit microcontroller capable of running at 10 million instructions per second. It was chosen for the following reasons:

Reasonable speed – 10 MIPS adequate for the control requirements of the system.

Adequate memory – 32 Kbytes of on chip program space which is more than is required for the system.

Low cost in comparison to competitive MCU's.

Future pin for pin compatible upgrades will become available allowing for easy integration into current design.

Compatible 'C' compiler available to program MCU with as an alternative to assembly language. This allows much easier solutions to process required equations and algorithms for the systems functionality.

Easy migration from previous microchip MCU's which experience and familiarity allows for quicker development.

The MCU comes from the same manufacturer of microcontrollers as the dsPIC60F3014 used in the DALC system but is from an older family. The reason for using an older and less powerful device is that it is adequate for the requirements it is designed to serve and, more significantly, a 'C' compiler is available to program the device with, removing the need to attempt floating point arithmetic using assembly language. This is particularly important in the context of the dual-channel temperature controller, which is based entirely in software. The reason the DALC system was processed in assembly was because there was no requirement for complex calculations – mostly a series of very fast switching and simple data manipulation to achieve the required frame rate, and the requirement in this system for high speed.

4.5.1. Basic MCU hardware setup

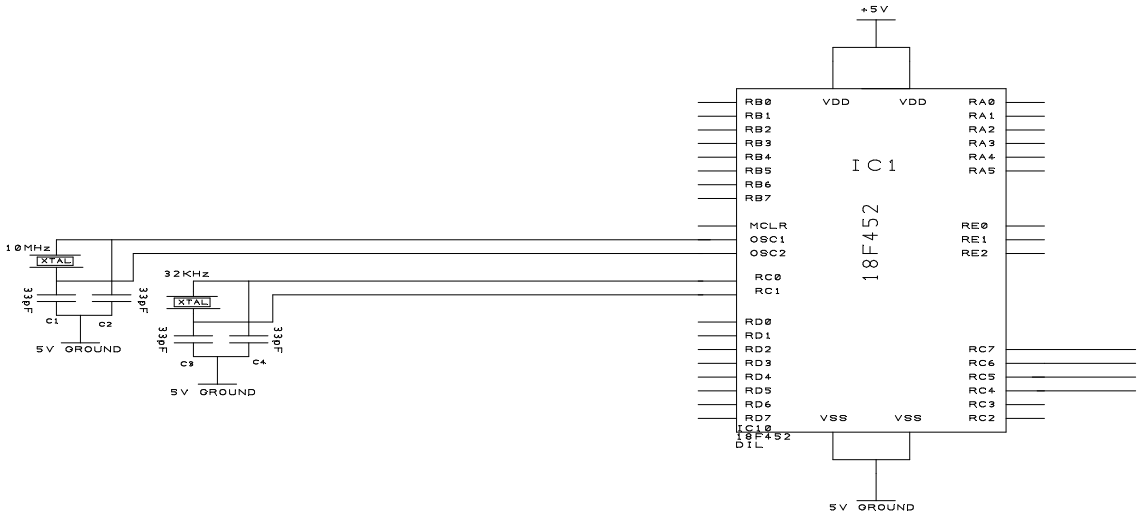

Figure 4.4.: Diagram of basic MCU hardware setup

The MCU is powered from the 5 V logic supply. The MCLR pin is pulled up to 5V to give a hardware reset at switch on.

The system clock for the MCU is derived from a 10 MHz crystal XL 1. XL 1 has two 33 pF capacitors connected from each pin to ground with both pins connected to OSC1 and OSC2 of the MCU with OSC1 being the oscillator input and OSC2 being the oscillator output. This 10 MHz is frequency multiplied by four by the on chip phase locked loop (PLL) to give a system frequency of 40 MHz which, divided by four internally, gives an instruction cycle of 100 ns. A 40 MHz oscillator can be connected directly between these two pins and bypass the PLL but using such high frequency crystals can cause RF problems and cause interference on other parts of the circuit.

On this system an additional crystal XL 2 is connected to the MCU. The timing capacitors for this part are 15 pF. The value of this crystal oscillator is 32.768 kHz which is required for the real time clock part of the system for data sampling/acquisition and control algorithms.

4.5.2 MCU and latch connections

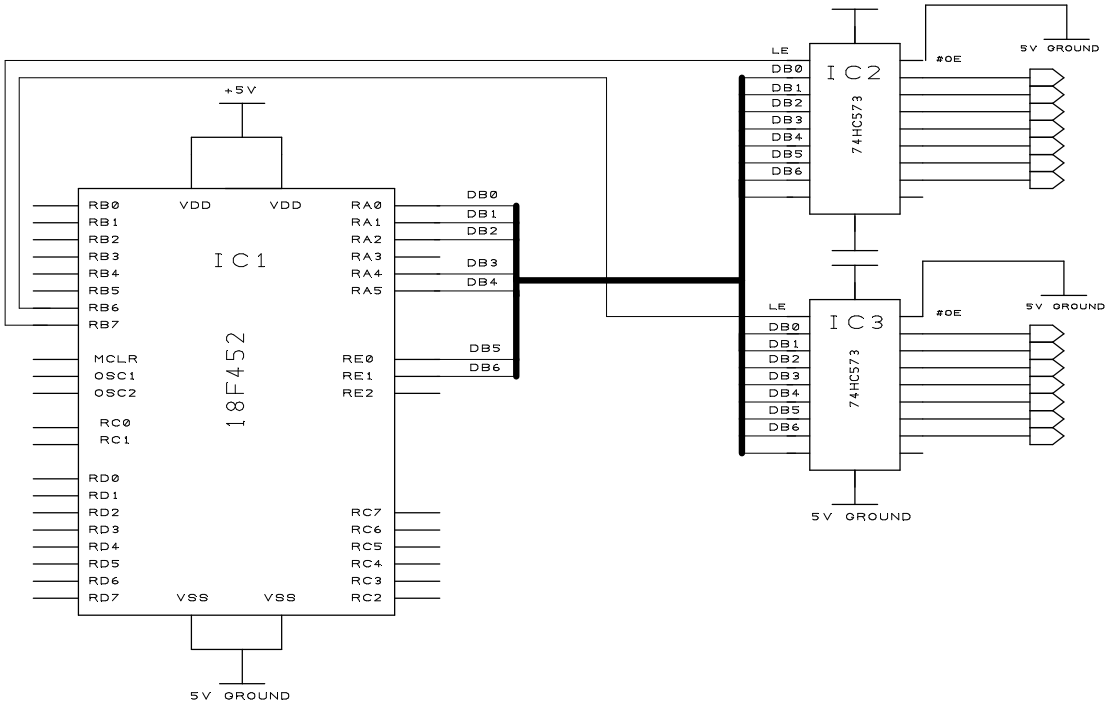

Figure 4.5.: Diagram of MCU and Latch connections

Both data latches are 74HC573 [7] devices which consist of eight inputs and eight latched outputs. The two data latches are used for port expansion for the MCU. The output enable pin is permanently tied to ground. In this format, when port RB7 goes high data from RA0,RA1,RA2,RA4,RA5,RE0,RE1 (DB0 – DB6) become latched on (latch1) IC2's data outputs. When RB6 goes high (DB0 – DB6) become latched on IC3's (latch2) data outputs.

The outputs from latch 1 are as follows:

LDB0 is the Q switch logic enable signal to the Q Switch driver.

LDB1 is the logic enable signal to the laser diode drive..

LDB2 and LDB7 form the logic direction control for channel one and channel two of the TEC drive respectively.

LDB3 is the reset control for the two support MCU's supplying the PWM outputs to the dual TEC drive.

LDB4-6 are the control lines for the AD7391 digital to analogue converter which produce the analogue control signal for the laser diode drive.

The outputs from latch 2 are as follows:

LDB0 is the logic control for the audible sounder.

LDB4 drives the laser On/Off panel LED indicator.

4.5.3 PWM Generation

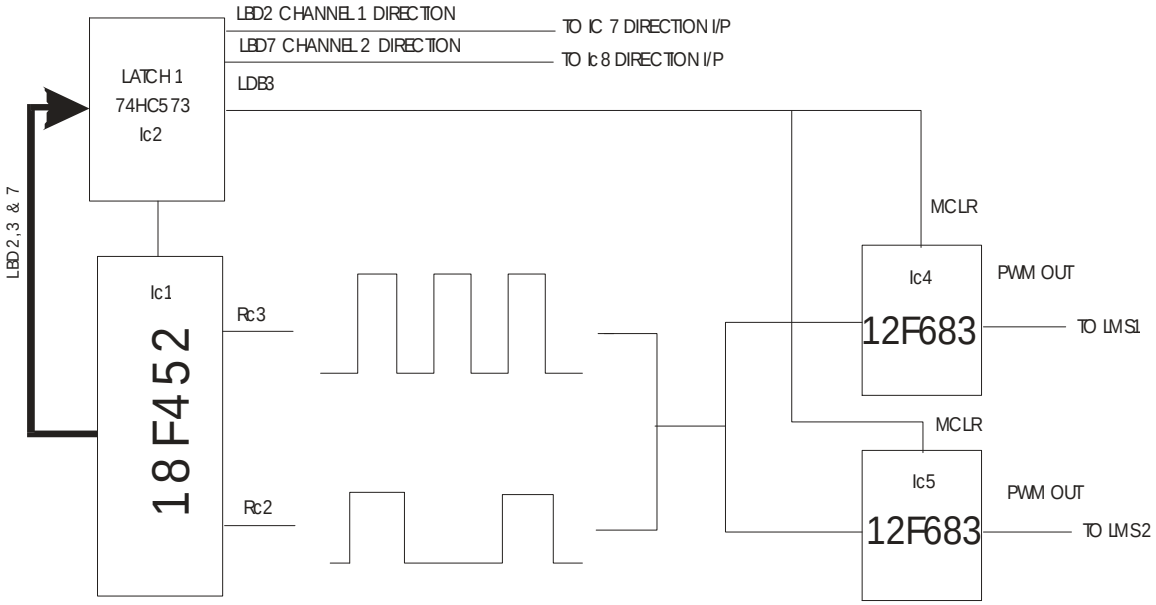

Figure 4.6.: Diagram of 2 wire custom protocol.

The TEC driver stage requires a PWM input signal proportional to the power required across the TEC. The advantage of driving TEC's in this manner is that the control signals don't suffer from noise and these signals are very simple to generate, and also remove the need for a dual-rail power supply, required by many linear output stage designs. In addition, PWM designs are inherently more efficient that their linear counterparts as their impedance is either very high or low, implying that very little power is dissipated in the output stage. The main disadvantage is that there are a finite number of levels of power in PWM control whereas in linear control there is no restriction. To achieve two PWM outputs to drive the dual TEC output stage, two support microcontrollers (IC 4 and 5) are embedded into the system. The support MCU's (12F683) [8] are also from the microchip family and are a cut down version of the main MCU. They were chosen for their compact size (8-pin DIL) and the fact they have their own on chip PWM driver modules. This was done because the main MCU only has one on chip PWM driver module. The two support MCU's communicate with the MCU by means of a two wire custom communications protocol. Latch 1 LDB3 is connected to the reset pins of these devices

and RC2 is connected to the assigned data pin 6 of both devices and RC3 is connected to the assigned pin 7 of both devices.

The power required to be sent to each TEC is calculated by two PID software loops in the main MCU. The value produced by the algorithms are in the range between -1000 and + 1000. The values -1 to -1000 heat the TEC and the values 1 to 1000 cool the TEC. The value 0 applies no power to the TEC. Any negative value will send the same value as it's positive counterpart except that the heat/cool logic signal to the appropriate TEC output stage will differ. To understand how the communication between the various MCU devices work it is important to understand that the two support MCU's have 10 bit PWM output modules. To keep the system well scaled the numbers produced from the main MCU are in ten bit format that is why the numbers produced from the algorithm are between 0 and 1023. The main MCU sends out the algorithm value in serial format along with 10 clock pulses with RC3 assigned as the clock pin and RC2 assigned as the data. The main MCU resets the two support devices via latch 1 LDB3. On reset the two support devices await the first clock pulse and when it arrives IC4 starts decoding the data. On the first pulse the IC4 checks whether the data is high or low, if it is high then the LSB of the 10 bit number is a '1' if it is low then the LSB is a '0', all the remaining bits of data are encoded in the same manner. As each bit of data is clocked in to the device the data bit is put into the PWM module. When 10 pulses are completely received and the data encoded the value in the PWM module is activated and the 10 bit algorithm value produced in the main MCU is represented in PWM format on IC4's PWM output pin which determines the power across the TEC via the LMS device. While IC4 encodes the first 10 pulses support IC5 is programmed to ignore the first 10 pulses and not encode any data. The next 10 pulses are encoded by IC5 with the value of the second PID loop value produced in the main MCU while IC4 doesn't encode these 10 values. IC4 encodes the next 10 while IC5 doesn't and so on.

4.5.4 Front Panel Hardware Interface

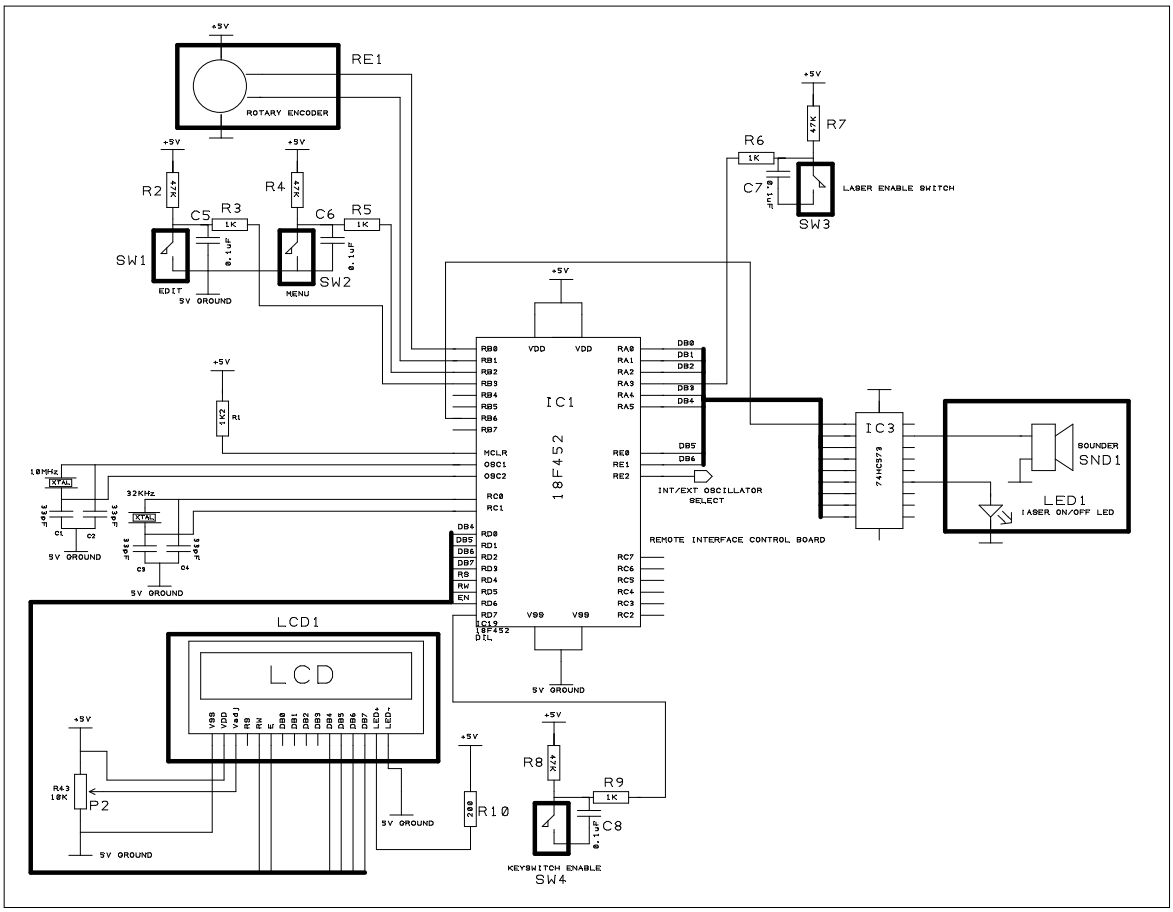

Figure 4.7.: Front Panel Hardware Interface

The four switches (Menu,Edit, keyswitch Enable and Laser Enable switch) are connected to the MCU's pins RB2,RB3,RD7 and RA3 respectively. They are all connected in the same manner with a 47 KΩ pull up resistor and a 0.1μF capacitor connected across the switch to 5 V ground. A 1 KΩ series resistor is connected to each pin to help prevent spurious signals. When any of the switches are pressed the corresponding port bit changes from a logic high to a logic low which the MCU detects and acts accordingly.

The rotary optical encoder [9] is a device which, when rotated produces 128 pulses per resolution. The encoder is supplied by the 5V rail and when turned produces quadrature-phase 5 V logic signals from its two output pins to the MCU's inputs RB0 and RB1. The MCU detects the edges of these signals to determine when and in which direction the encoder is being turned.

The alphanumeric LCD is a 4 line x 20 character. Hitachi compatible module [10] and communication is achieved to the MCU by 3 control lines and 4 data lines. (Hitachi standard 4 line communication) [11]. Port D bits 0 to 3 are connected to the high order data bit lines DB4-DB7. RS,RW and Enable are connected to RD4-RD6 respectively. The 4 line display was chosen to allow more information feedback as opposed to a 2 line display. Important parameters are displayed on the LCD such as temperature, laser diode current and PID constants allowing for ease of use whether in setup mode or monitor mode. A 10 KΩ potentiometer is connected across 5 V and ground with the wiper being connected to the V_{adj} input on the LCD module. This allows for contrast adjust of the panel. A 200Ω resistor is connected with the internal LED in the LCD panel. This is the backlight that allows for character viewing in transparent mode[12].

A buzzer is controlled by the MCU via latch 2, as is the laser on/off LED. The buzzer gives audio feedback in certain situations such as error warnings, switch press confirmation, rotary encoder change etc. The laser on/off led is self explanatory and gives indication as to the status of the laser diode.

4.5.5 Dual channel TEC Drive

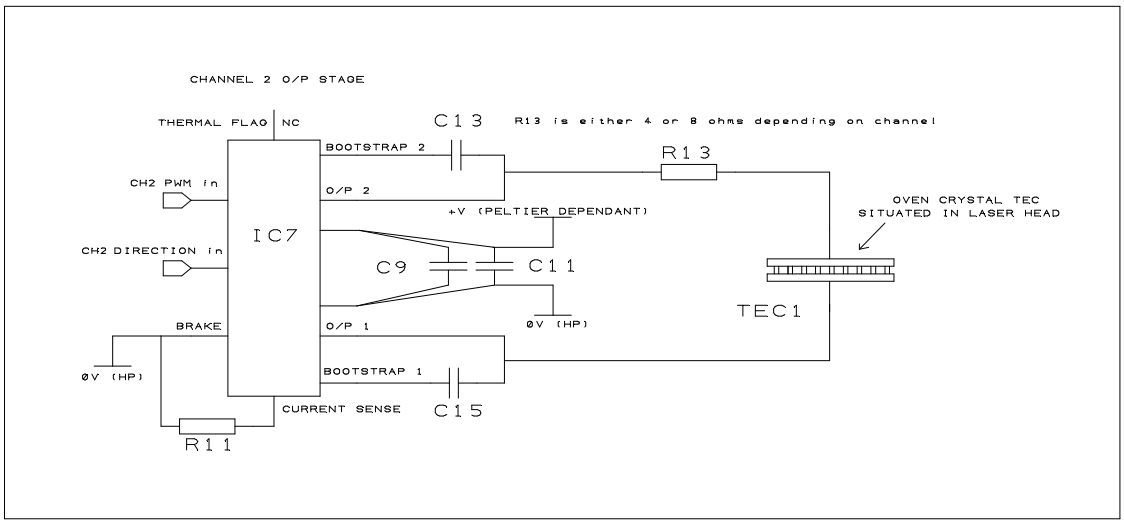

Figure 4.8.: Diagram of one channel TEC drive circuit.

The laser diode TEC and nonlinear crystal TEC are driven by an output stage based around the LMD18200 H-bridge. The device is capable of supplying 25 W of power to its loads which in this case are the TEC's. The laser diode TEC is a 8 V, 2 A device and the nonlinear crystal TEC is a 4 V,1 A device , both of which are situated in the laser head. The laser diode TEC is supplied from the 12 V rail which requires a series 4Ω resistor with the laser diode TEC and a series 8Ω resistor with the non-lineear crystal TEC. The LMS has a PWM input which are supplied by the two 12F683 devices. The direction pins are controlled by indirectly by the main MCU via latch 1 LDA2 and directly by RB5. When a logic high signal appears at H-bridge the TEC cools the load and when a logic low appears the TEC heats the load. The PWM supplied to the device from the support MCU's is in a 10 bit format (0 – 1023). A 2000 μF capacitor along with a 1μF capacitor are connected across the 12V high current supply close to the device to suppress supply spikes due to the fast switching of high current pulses.

4.5.6 Q Switch Driver Associated Electronics

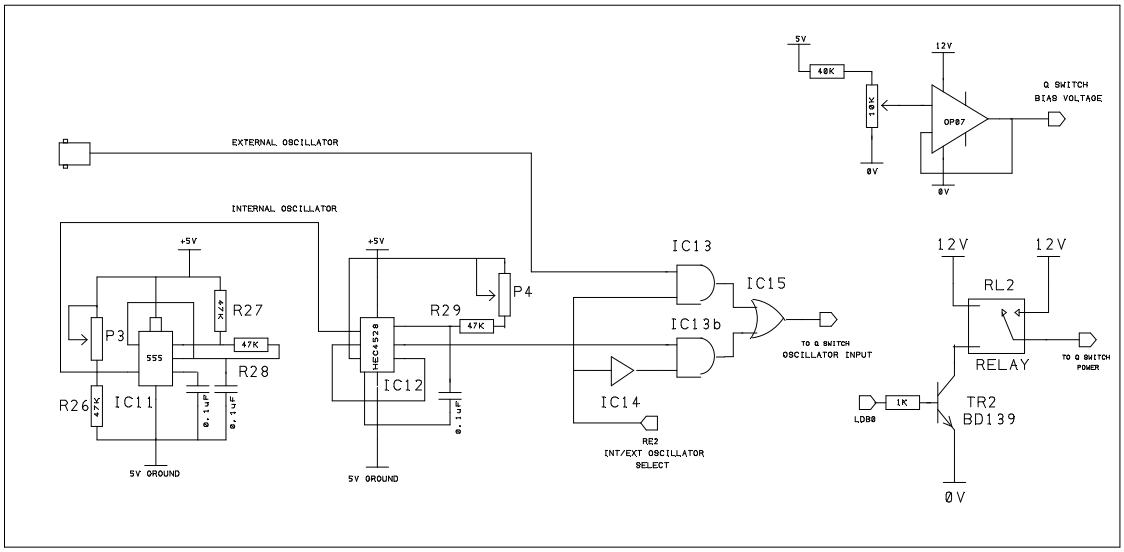

Figure 4.9.: Q Switch Driver Associated Electronics

The Q switch associated electronics supply the various signals required to drive the Q switch driver appropriately. The power to the Q switch driver is controlled electronically by a logic signal from LDB0. This signal switches the transistor TR2 which power the relay (RL2). The normally open contacts then close supplying power to the Q switch driver module. The 555 timer produces the

required 300-500 kHz signal which can be varied by P3. The output of this oscillator are fed into the monostable multivibrator which produce the required pulse of between 100 ns and 1 uS. The variation can be achieved by adjusting P4. A logic signal from port RE2 dictates whether it is this internal oscillator or whether an external oscillator is fed into the or gate which is fed to the Q switch driver. The external signal, derived from an external signal generator or scan controller IAD system as necessary, is fed into the system via a rear panel mounted BNC connector.

4.5.7 Laser Diode Drive and DAC

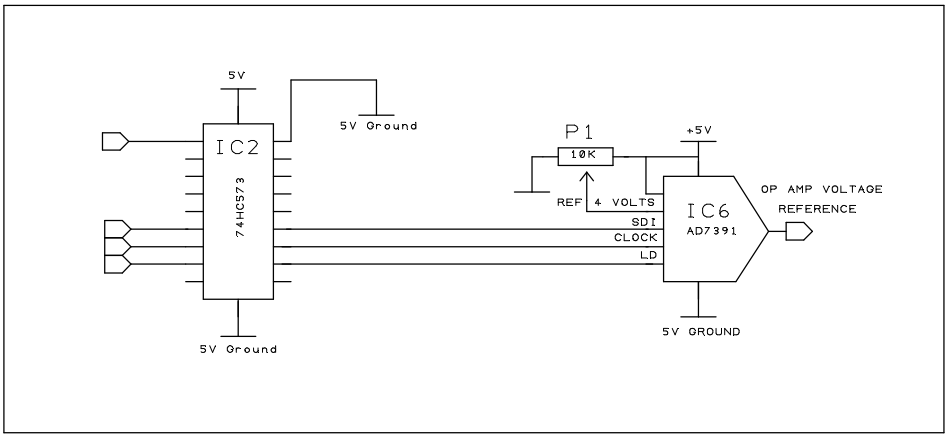

Figure 4.10.: Schematic of DAC connections.

The AD7391 (IC6) [13] digital to analogue converter produces the analogue signal for the laser diode drive. It was chosen for the system because of it's adequate resolution (10 bit) and speed along with it's simple serial interface. (Standard SPI protocol [14]). The potentiometer sets the reference voltage to 4.096 V allowing for 4 mV resolution per bit. (4.096/1024 bits). The linear constant current output stage has a transfer characteristic of 1 A/V and therefore the maximum current that can be called for by the MCU is 4.096 A in 1 mA increments – far in excess, in both amplitude and resolution, of what is required in this application. Therefore, the resolution was reduced further in software to 100 mA adjustment increments and the maximum allowable current user presentable up to 3.5 A. The three communication pins (The SDI,Clock and LD) are controlled by the MCU indirectly via Latch 1 LDB4-LDB6.

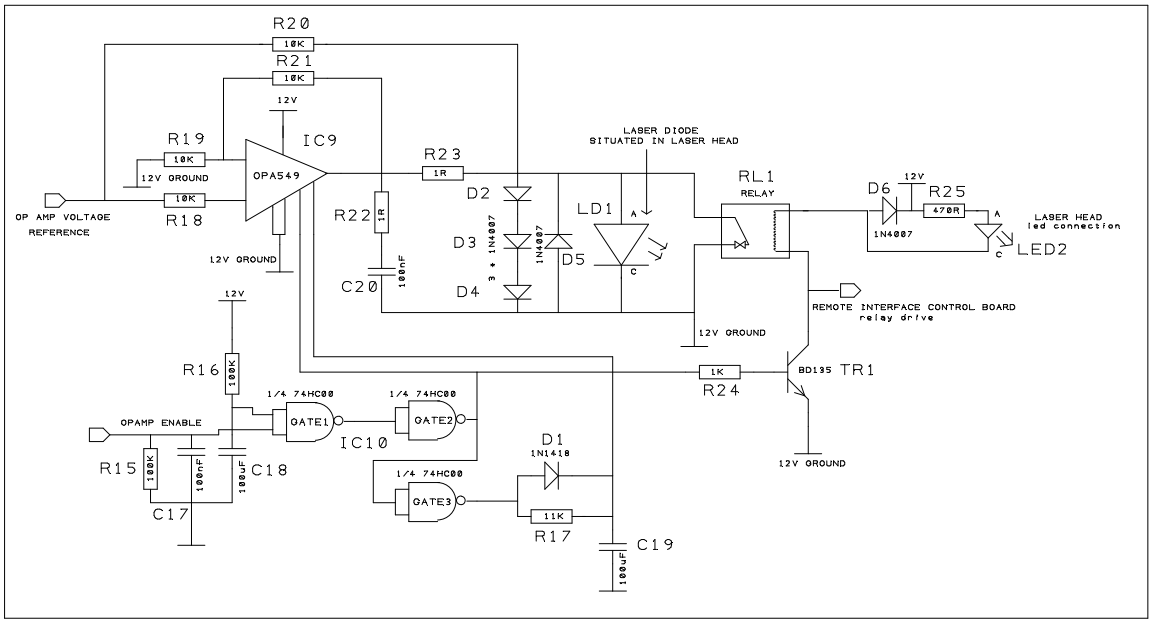

Figure 4.11.: Laser diode drive schematic

Constant current through the laser diode is achieved by the constant current stage revolving around the OPA549. Various hardware safety features are implemented into this section to give extra protection to the expensive laser diode. A high signal is applied to the op amp enable stage when the two inputs become high to the first NAND gate (the other pin is pulled high with the RC network (R16 and C18.) The capacitor C17 suppresses any noise to prevent spurious logic signals. If both inputs are logic high at gate 1 the output from the gate is low. With logic low being fed into gate two and gate three which are configured as inverters, the outputs are high at gate 3 and low at gate 2. The logic high from gate 2 is connected to the enable input of the power op amp and also fed into the R24 connected to the base of transistor TR1 which switches the transistor on. By switching the transistor on the relay becomes energised and opens the normally closed relay contacts. This opens the short across the laser diode allowing current to flow through the it. The logic low at gate 3 discharges C19 of the RC network of R17 and C19 giving a slow turn on of approximately 3 seconds to protect the laser diode from thermal shock and electrical transients. When capacitor C19 is fully charged up the resistor value of R17 limits the current flowing out of the op amp to 3.2 amps maximum. When the enable input and the Ilim input are set current will flow through the ballast resistor down through the laser diode. The amount of current flowing through the ballast resistor and the laser diode are depending on the voltage supplied to the op amp reference input which is supplied by the DAC. The 1Ω and 100 nF RC series network at the output of the op amp help prevent oscillation which can easily occur in high powered op amp devices.

The three series 1N4001 forward biased diodes ensure the maximum voltage across the laser diode will not exceed ~1.8 V. The reverse bias diode D5 prevent any negative spikes damaging the laser diode which would be clamped to -0.6V should this voltage be exceeded.

4.5.8 Remote Interface Control Board

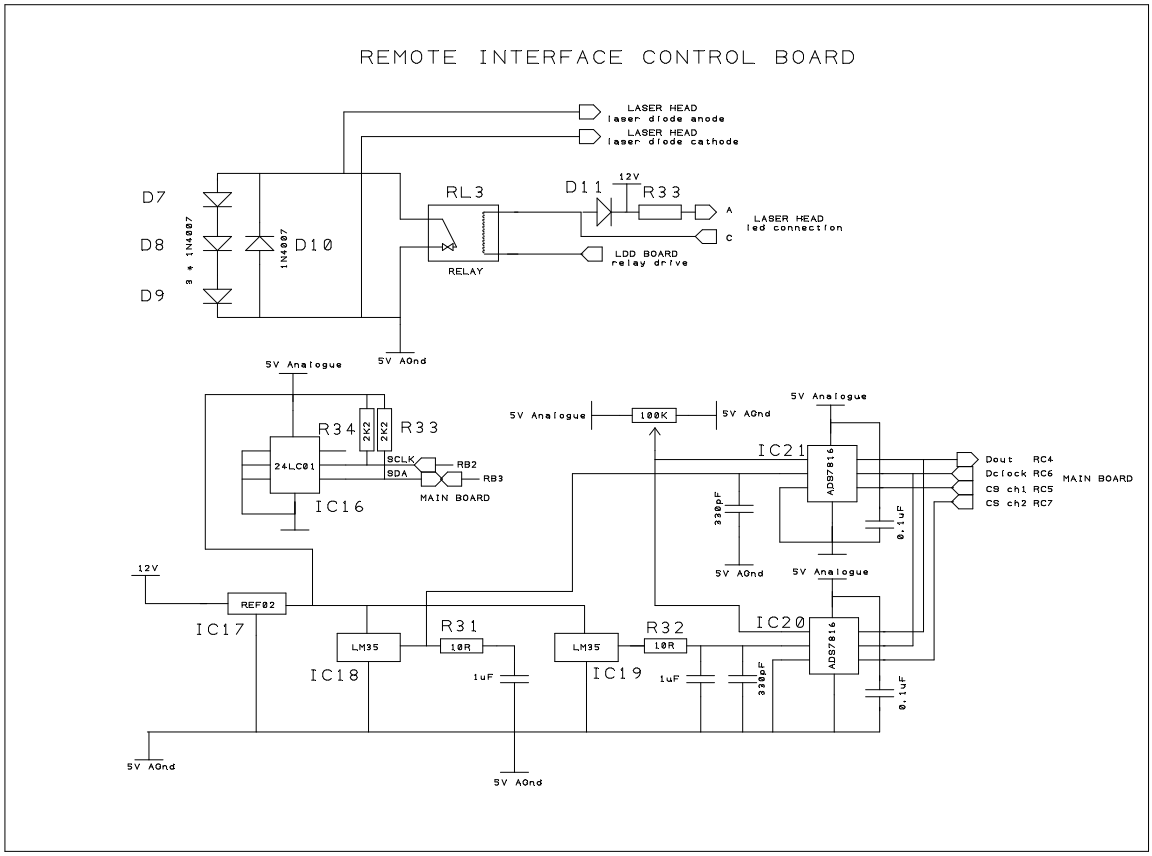

Figure 4.12 : Schematic of remote interface control board.

The RICB is situated in the laser head. This board is designed for low noise because of the required low level signal measurement for accurate temperature to be sensed from the two TEC loads. To measure +/- 0.025 of a degree with the semiconductor sensors chosen (10 mV/degree C) voltage levels of 0.25 mV have to be measured. Even allowing for low noise precautions to obtain maximum accuracy, 50 samples are taken for each channel and averaged out to give a very stable reading.

The 5 V supply to the low noise circuit is supplied from the REF02 [15] which was chosen for its low noise capability and it also able to supply sufficient current to the rest of the RICB circuit (15 mA).

The two LM35DZ [16] sensors (IC20 and IC21) were chosen because of their excellent stability and accuracy as importantly their linear degree Celsius response making post-processing of the digitised signal unnecessary as would be the case for a thermistor. The sensors are located remotely in their respective mounts and are thermally connected to the two TEC's loads. The output from each sensor has a series RC network connected from this to ground. This allows for the sensor to drive a capacitive load which is required since the sensors are connected off board via connection wires and hence introducing unwanted capacitance. The sensor outputs are also connected into their own analogue to digital converter (ADC) reference input. The potentiometer (PX) sets the reference voltage on the DAC's which is set to 1.024 V which results in a 100 mV input signal decoding as a value of 10 degree celcius. Each DAC is decoupled by a 0.1μF capacitor. The inverting input of both DAC's are connected directly to the low noise ground. A 330 pF capacitor is connected between the non inverting input and ground to suppress any noise from the remote sensors. The output communication between the main MCU and each DAC is in SPI compatible mode [14]. The two DAC's share the two communication lines – the data ouput and the clock input. They have their own CS/SHUTDOWN communication lines. The main MCU decides which DAC it was to communicate with and enables it's CS line and disables the other one. The 24LC01B [17] EEPROM stores all of the various parameters such as PID constansts, setpoints etc. required to be stored in a non-volatile manner for the system. The EEPROM is situated in the laser head so each head has its own parameters and can be easily switched between systems without the need for re-tuning. The EEPROM communicates between the main MCU via standard I2C protocol.[18]

The extra rectifying diodes are of an identical nature to the protection circuitry situated in the laser diode drive for the laser diode. This part of the circuit is connected in parallel to the other part to simply add extra protection. The remote wires from the laser diode are fed into this part and onto the laser diode which is situated in the head. The relay is RL3 is present to protect the diode when the laser head is detached.

4.6 Software Used In the LMS System

The software used in the development of the LMS system were:

MPLAB – An integrated development environment (IDE) designed by Microchip specifically for their brand of MCU's.

Elnec – Software designed to transfer compiled hex and assembly files to the target processor via a programming device.

HI-TECH PICC-18 – A C compiler designed for integration into MPLAB to allow C programming of PIC 18F MCU devices within the environment.

4.6.1 Interaction of Software

The interaction of the software in the development of the main MCU in the system was that the PICC-18 compiler becomes embedded into the MPLAB IDE making use of the excellent IDE and the C compiler. The C compiler is supplied with it's own IDE but due to personal preference and familiarity the MPLAB version was used. The MPLAB version has it's own simulator embedded into the environment which was ideal for simulating small blocks of tricky code. When a program was compiled the resulting hex file was imported into the ELNEC software and after setting up basic programming parameters the target processor becomes programmed. In reality this process was done hundreds of times before the final version of code was programmed. This is because an easier way to develop a system is to write small blocks of code and check its functionality within the hardware. Sometimes the code doesn't perform to expectations and has to modified and reprogrammed. When other pieces of code are written it all has to interact with other code and on occasion this doesn't happen as envisaged. This modular approach to development can appear slow and cumbersome initially but can save much time and heartache at a later stage.

The interaction of the software in the development of the two support MCU's was of a similar fashion except that the C compiler was not used. This was because the support MCU's were programmed in assembly language as opposed to C as there was no requirement for floating point arithmetic in their

functionality. Their objective was to check I/O ports and follow simple instruction to construct a 10 bit number and setup the on board PWM module accordingly.

4.6.2 The C Compiler

As previously mentioned in section 3.6 the compiler used in developing the software for the main MCU was the HI-TECH PICC-18. This compiler was chosen after research was done on all competitive compilers. Figure 3.6 summarises HI-TECH's advertisement of the compiler. One main advantage is the ANSI C compatible. This allows for other blocks of C code to be seamlessly imported from other C environments. One huge advantage of using a C compiler as opposed to assembly language is time spent in development particularly when writing mathematical formulae. Even basic program flow becomes much quicker and less tedious. In time gone by some embedded programmers would refuse to use C compilers believing to be more in control writing assembly as C compilers could never produce as efficient code as they could program in assembly format. However, in more recent times C programmers for microprocessors and microcontrollers have improved significantly thus HI-TECH claiming their compiler equals or betters assembly code in terms of memory efficiency and system speed

HI-TECH PICC-18™

HI-TECH PICC-18™ is a powerful C compiler for the Microchip PICmicro® PIC18 family of microcontrollers. HI-TECH PICC-18 upholds the robust and efficient tradition of a long line of PICmicro compilers from HI-TECH Software, delivering unrivalled code density combined with excellent reliability. Tightly tuned to the PIC18 architecture, it allows firmware development in a fraction of the time, but with no greater use of RAM or ROM, required for conventional assembly language programming.

HI-TECH PICC-18™ Compiler Features:

- ANSI C - full featured and portable
- Efficient - equals or betters hand-written assembler code
- Reliable - mature, field-proven technology
- Modular - includes full object code linker and library manager
- Cost-effective - productivity gains rapidly repay purchase cost
- Compatible - integrates into the MPLAB® IDE, MPLAB ICE2000 and 4000, ICD2 and most 3rd-party development tools
- Library source - for standard libraries and sample code for various peripherals and applications
- Complete - includes macro assembler, preprocessor and one-step driver

HI-TECH PICC-18 allows you to concentrate on developing your application, and eliminates much of the detailed, low-level coding effort. Our commitment to quality customer service ensures that you will have access to timely and accurate technical support when needed.

PICC-18 is constantly updated to support new PICmicro devices as they become available, and the ANSI C basis of the compiler protects your code investment.

Figure 4.13.: Advertisement of HI-TECH PICC-18 by HI-TECH [19]

4.6.3 Flowcharts of code execution

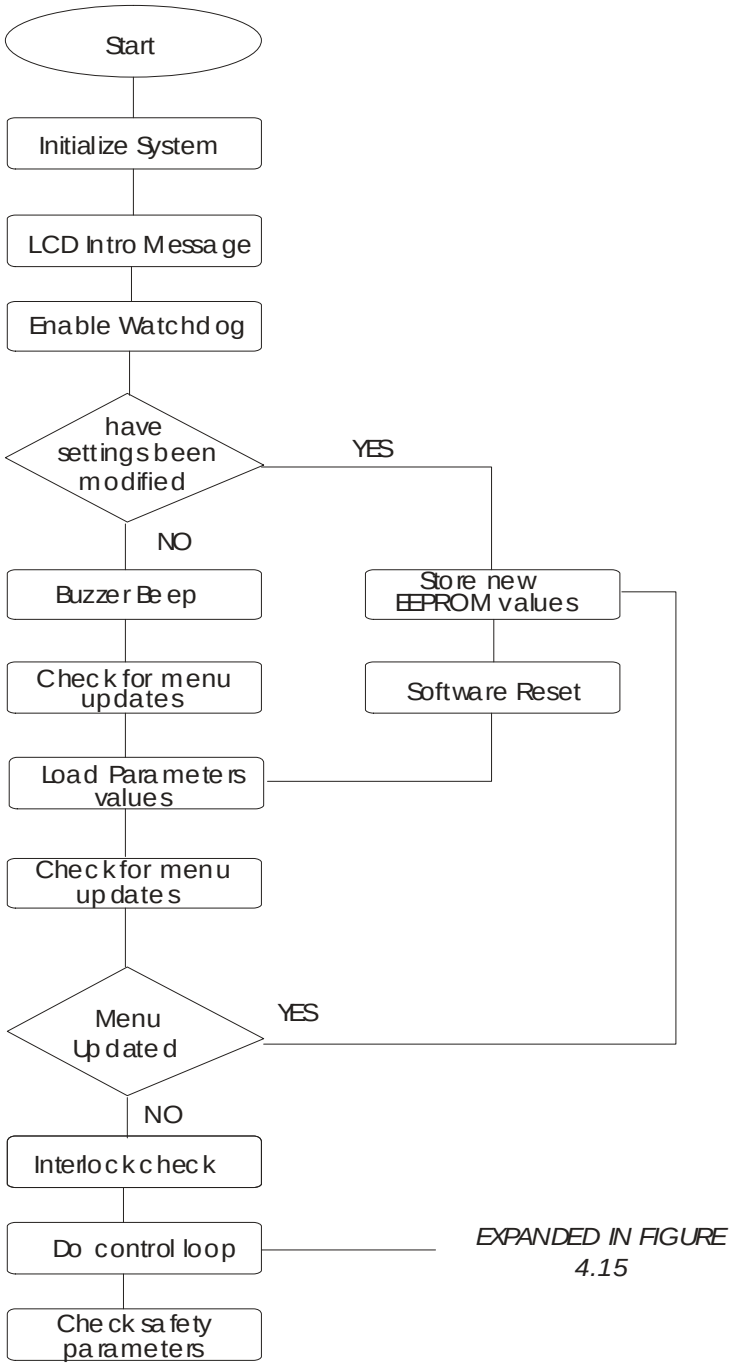

Figure 4.14 : Flowchart of LMS code execution

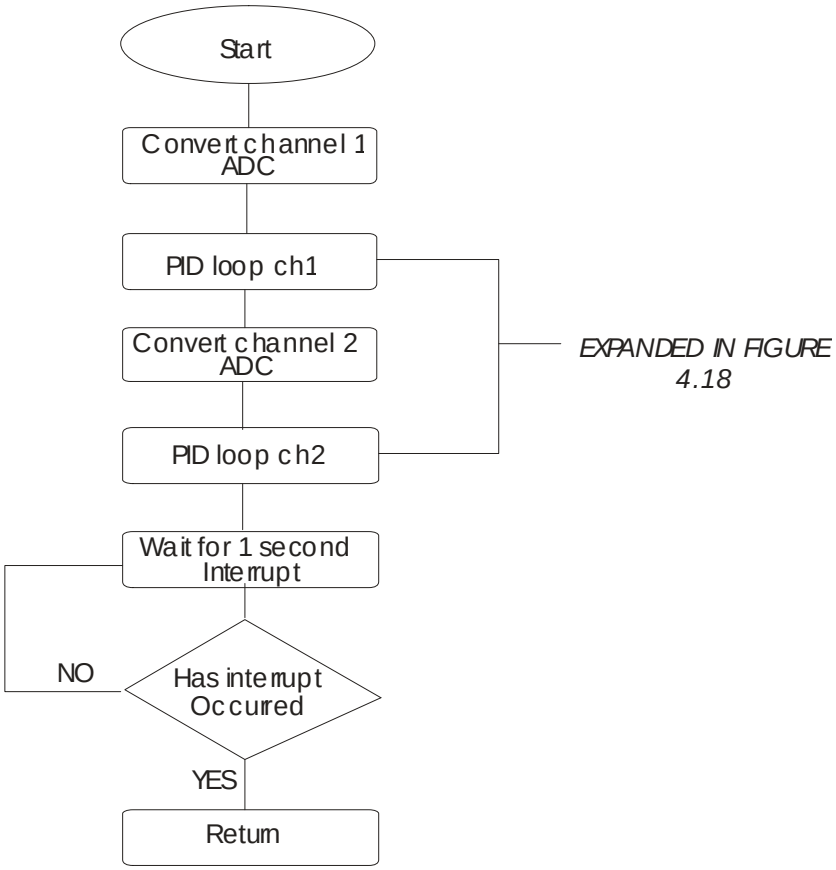

Figure 4.15 : Flowchart of LMS control loop code execution

4.7 PID Controller

A proportional-integral-derivative (PID) controller is a closed control loop that is regularly used in control systems for a wide variety of tasks controlling things like temperature, gas pressure, various motors etc. It is sometimes known as a three term controller because of the PID parameters. The basic theory of operation of a PID controller is that a desired set point (in this case a temperature set point) is referenced into the system. The actual temperature is measured and then fed back and compared to the set point. The difference between the set point and the actual temperature is called the error value which is fed into the system and processed by the PID variables which adjust the output to reduce the error. This would continue until the error value is zero meaning the temperature is at the required set point. Any fluctuation in temperature on the load (say possibly due to ambient/system temperature variations, wind currents etc) the PID system should react quickly and stabilize the error value to zero.

The stability of the PID system and its reaction times are dependant on the tuning of the PID parameters which will be covered in section 4.5.4

The purpose of a general closed control loop is the automation of a human operator continually reading and adjusting accordingly a measured value against its set point attempting to keep the system stable.

A control loop generally has three parts.

1. A sensor measuring the process to be controlled.
2. A decision making process.
3. An output stage acting upon the decision making process.

A general control system with these parts highlighted is shown in figure 4.16

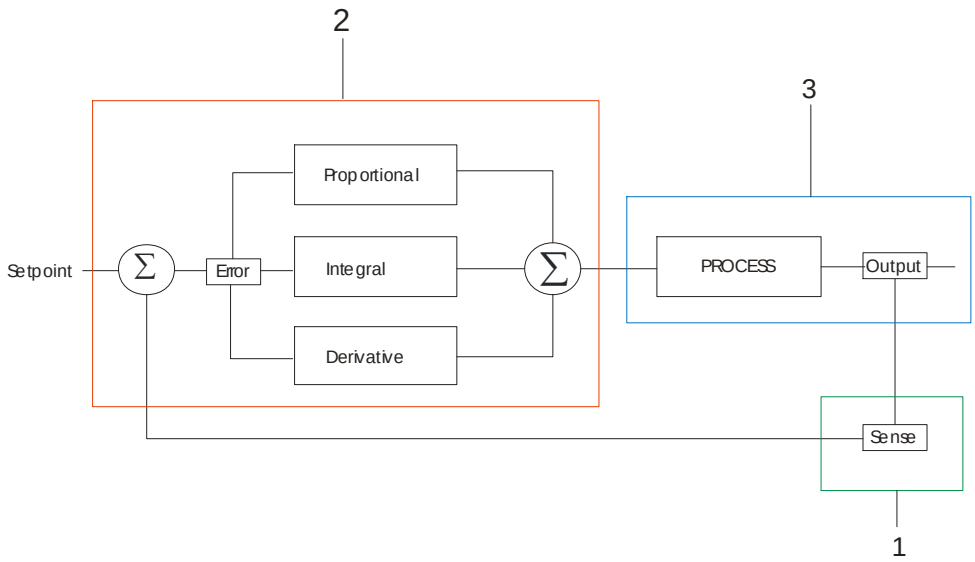

Figure 4.16.: Diagram of a PID closed control loop

In the TEC PID system the basic parts are as follow.

1. Semiconductor temperature sensor connected to the thermal load.
2. An MCU deciding what action to take with the measurement in the form of a software controller PID algorithm.

3. A PWM output stage adjusting the drive (if necessary) to the load.

4.7.1 TEC Control Loop

The basic parts of the TEC PID system are shown in figure 4.17.

The box highlighted by point X shows what part the MCU plays in this closed loop system with an algorithm to calculate the set point and temperature difference, calculate the proportional, integral and differential components and sum the total. The MCU then adjusts the PWM drive accordingly which is then connected to the PWM output drive.

The output drive supplies a high current PWM signal to the TEC which is connected to a thermal load. The sensor voltage reads a value which is then converted from an analogue

signal into a digital to signal which is then fed into the MCU to start another cycle.

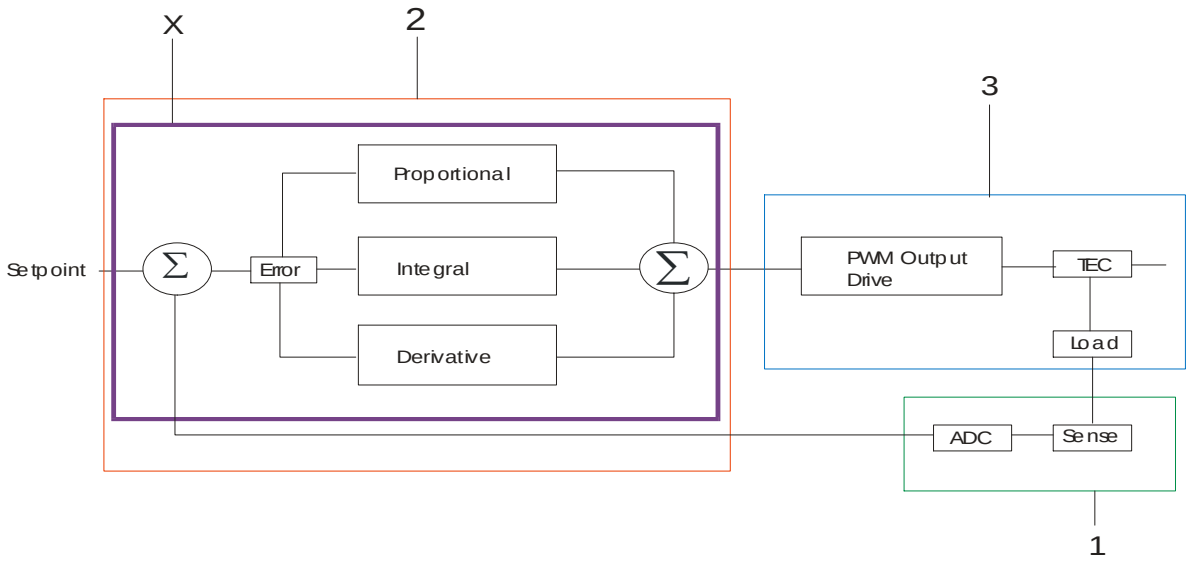

Figure 4.17.: Diagram of TEC PID closed control loop

4.7.2 Digital PID Loop

A flowchart showing how the digital PID loop is implemented is shown in figure 4.18. The current temperature value is taken then the current set point. The set point is then subtracted from the current temperature to produce an error value which is used in all three PID terms as follows:

$$\Pr oportional(P) = (A * E)$$

$$Integral(I) = B(E + Etotal)$$

$$Differential = C(E - Eprevious)$$

$$Output = P + I + D$$

The proportional term is calculated by a constant A multiplied by the error. The Integral term is calculated by multiplying a constant B and the current error value plus the total previous error total and the differential term is calculated by a constant C and the current error minus the previous error which calculates the rate of change. This is the algorithm in its simplest form and additional parts were implemented into the final C code such as safety features like temperature limits etc. to protect the laser diode and crystal.

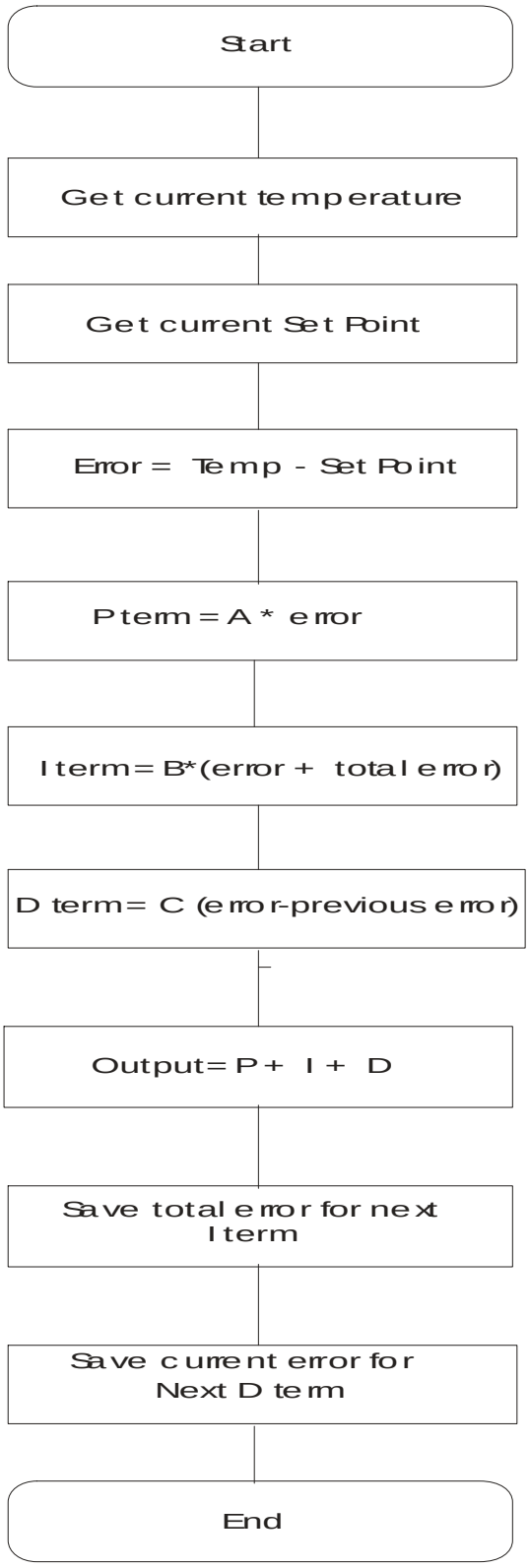

Figure 4.18.: Flow chart of the digital PID loop

Here is a brief explanation of what each term contributes.

Proportional- Works on the immediate error, the error is multiplied by constant A. If too much proportional is applied then large overshoots and oscillations may occur, if there is too little proportional the temperature may struggle to reach its set point. Ideally, the proportional should be able to reach the set point in an acceptable time and settle with just a small amount of steady state error.

Integral- works on a history of the past. If too much integral is applied then the system may go into a state of oscillation, if too little is applied the temperature may take a long time, if ever, to reach its set point and react slowly to temperature changes.

Differential- Calculates the rate of change of the system error which helps predict how fast the temperature is approaching the set point and can reduce overshoot.

Figure 4.19 shows some responses of a typical PID feedback system and how using the various parameters alter the response.

4.8 Tuning Methods of a PID System & System Performance Results

Depending on system requirements control systems can be set up to run with only P, PI, PD or PID. A proportional only system could be used if temperature accuracy isn't a critical requirement, PI can be used if temperature accuracy was critical but the time to reach stability was required to be as quick as it could be, PD can be used with a similar response to P only but with less or little overshoot and PID can be used for optimum performance. Tuning of these parameters is critical for best performance whether it be from a mathematical approach or a standard manual approach. There are many ways to manually tune a PID system to produce a desired result which can in most cases be of desired accuracy. A valid way which was tested in this system is to set a proportional value so the rise time is of sufficient speed. Once that has been resolved add enough differential to eliminate overshoot and leave a small steady state error and then finally add enough integration to reduce the steady state error.

This method works well and results of the PID manual tuning of the crystal oven (with a set point of 50 degrees Celsius) are shown below in figure 4.20. (The laser diode temperature can be tuned in an identical manner).

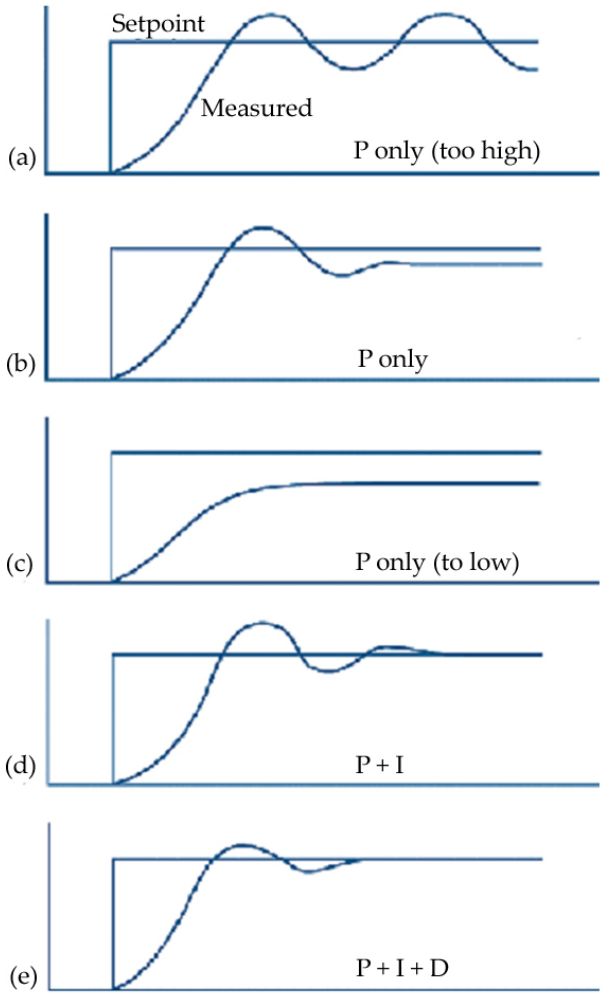

Figure 4.19: Diagram of a PID closed control loop [20]

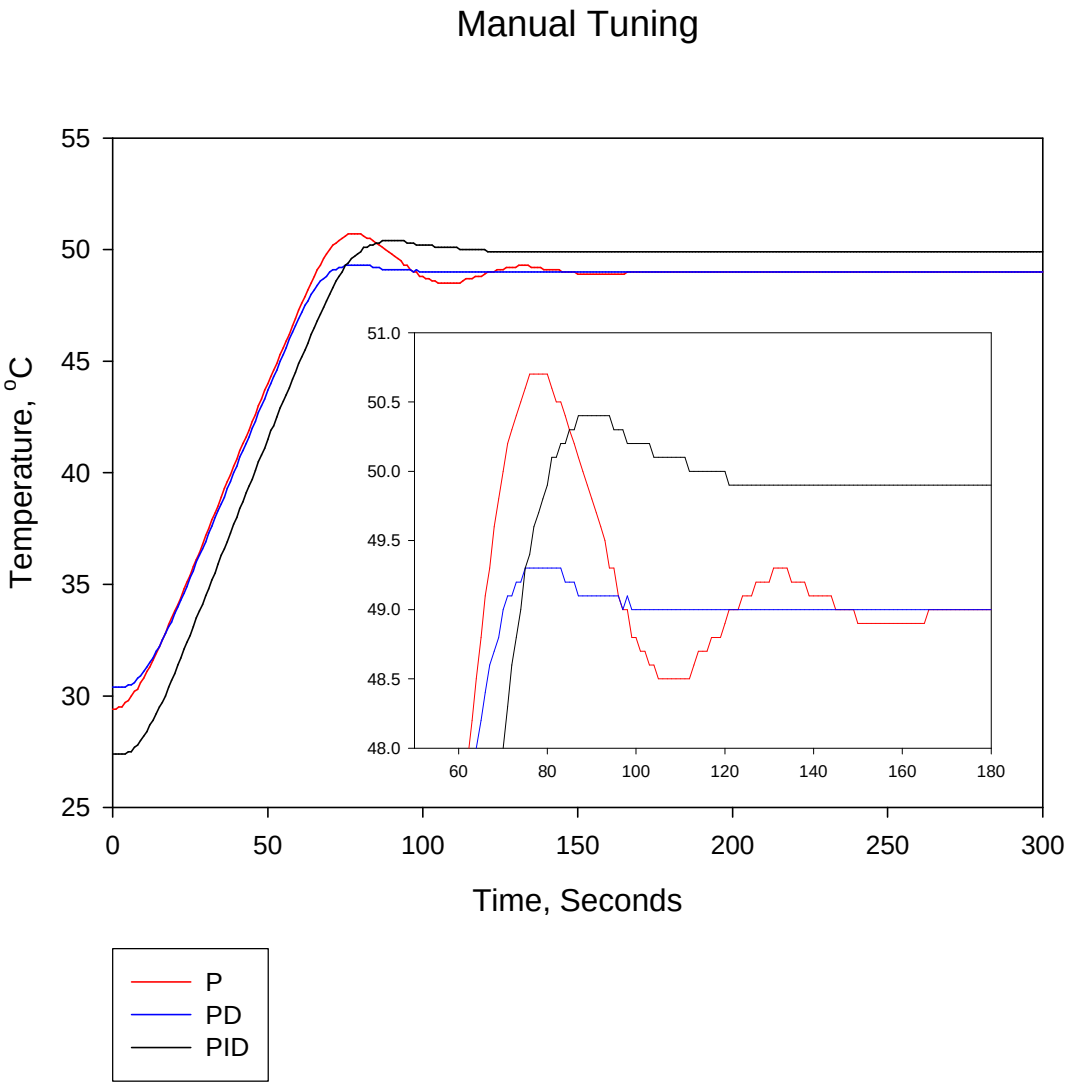

Figure 4.20.: Graph of manually tuned system

The red trace shows the proportional only response, the blue trace shows the same proportional value with a differential added and the black trace shows the response of the system with proportional, integral and differential. The PID response shows a settling time of about 120 seconds is adequate for wavelength change in the OPO system. The system was then challenged with a set point step response going from 50 degrees Celsius to 40 degree Celsius to see how it would react under real life changes in set point variances. The results are shown below in figure 4.21.

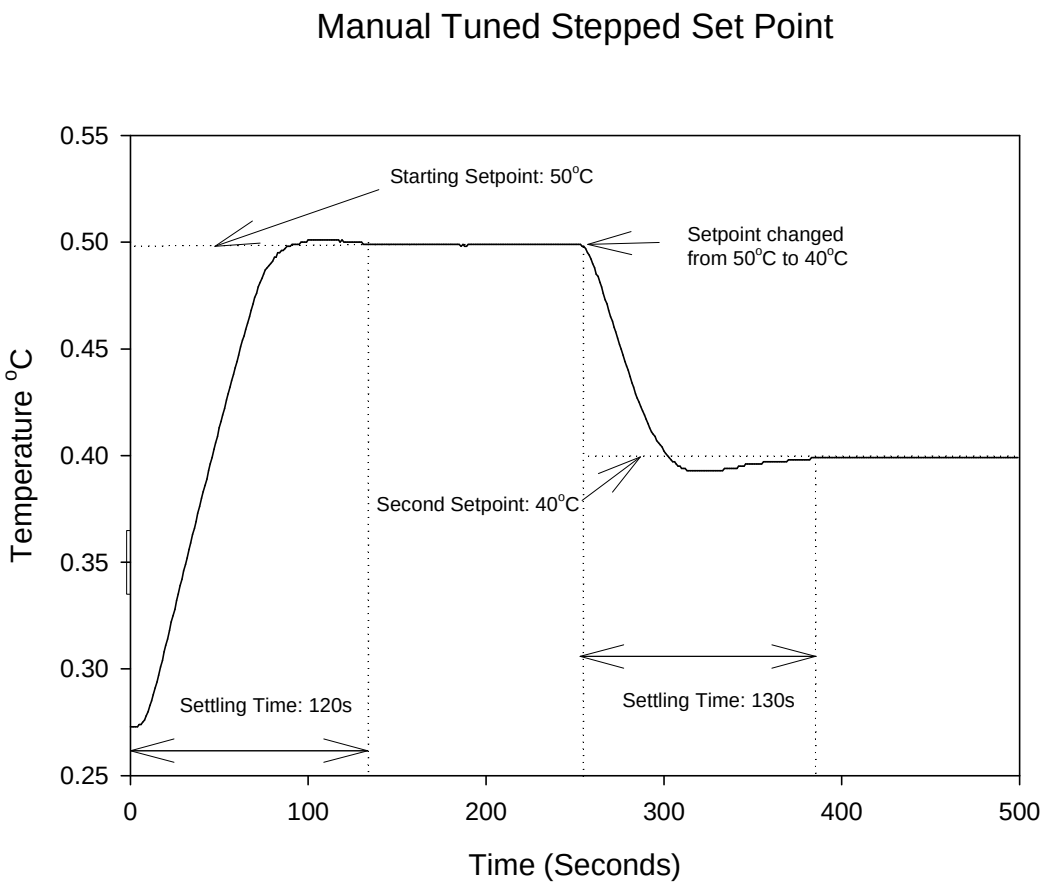

Figure 4.21.: Graph of set point change response of manually tuned system

The results from the set point stepped response show that the temperature controller reacts well to set point change. The slight overshoot occurring on the rise time is similar to the undershoot on the fall time. A noticeable point from the graph is the TEC's ability to heat the oven (22 degrees Celsius in 120 seconds, ie 0.183 degree Celsius per second) is much greater than its ability to cool the oven (10 degrees Celsius in 130 seconds, ie 0.076 degrees per second). This can be thought of strange considering room temperature assists with pulling the temperature down towards room temperature. However, this is due to the heat generated by the inefficiency of the TEC contributing to useful heating of the oven block when it is being driven above room temperature.

Obviously in some situations a more mathematical approach is required to ensure optimal performance and stability. One popular method of tuning a PID system in this manner is the *Ziegler-Nichols open* loop method which works by testing out the thermal characteristics of a particular load by testing it in open loop mode with a stepped response. From this response there are equations that can be used to

tune the system in closed loop mode for optimal performance. However, since the open loop test requires a stepped response of some stable value to 100 percent of output drive which would set the oven temperature to nearly 200 degree Celsius (due to a very low thermal mass) this method was avoided to prevent damage to the TEC. There is another method which was more suitable for this tuning experiment called the *Ziegler-Nichols closed* loop method. This involves increasing the proportional gain without any integral or differential until there is continual and repeatable oscillation. Figure 4.22 shows the proportional only value at 130 and the oscillations are nearly repeatable but with some distortions. This was increased until the oscillations became repeatable which was with a proportional gain value of 180. This value is called the ultimate gain which is then used in calculating the a,b and c constants required for putting into the digital algorithm. This response is shown in figure 4.23.

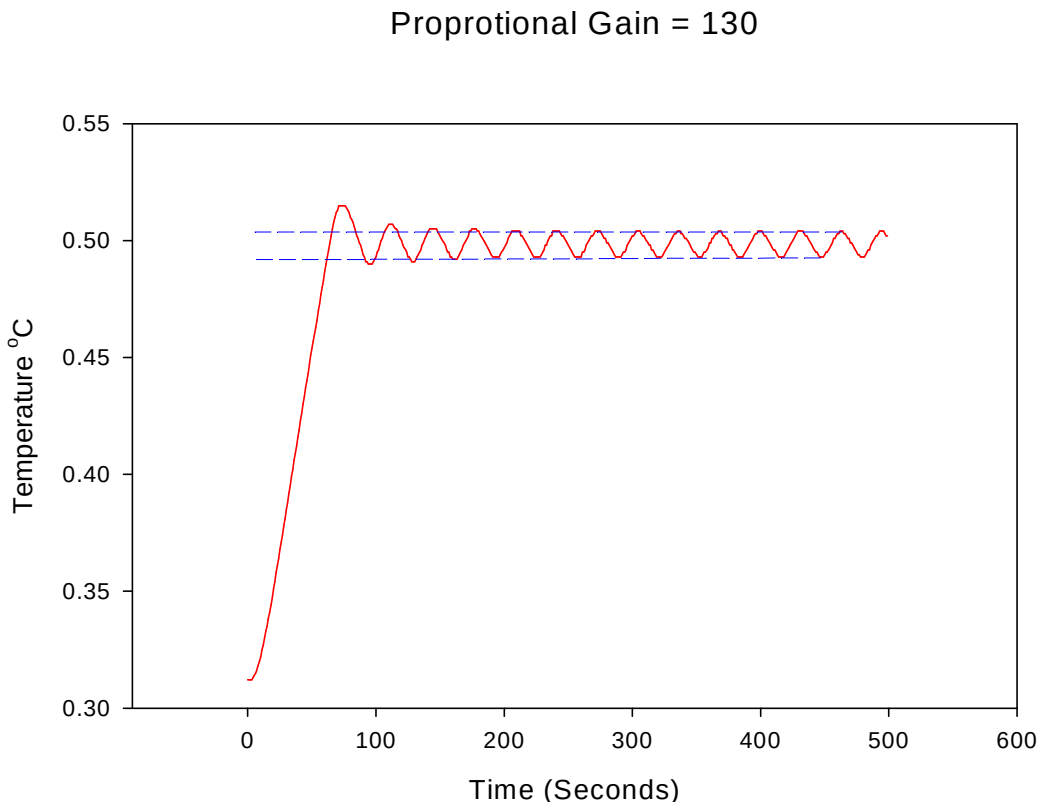

Figure 4.22.: Graph of proportional gain=130

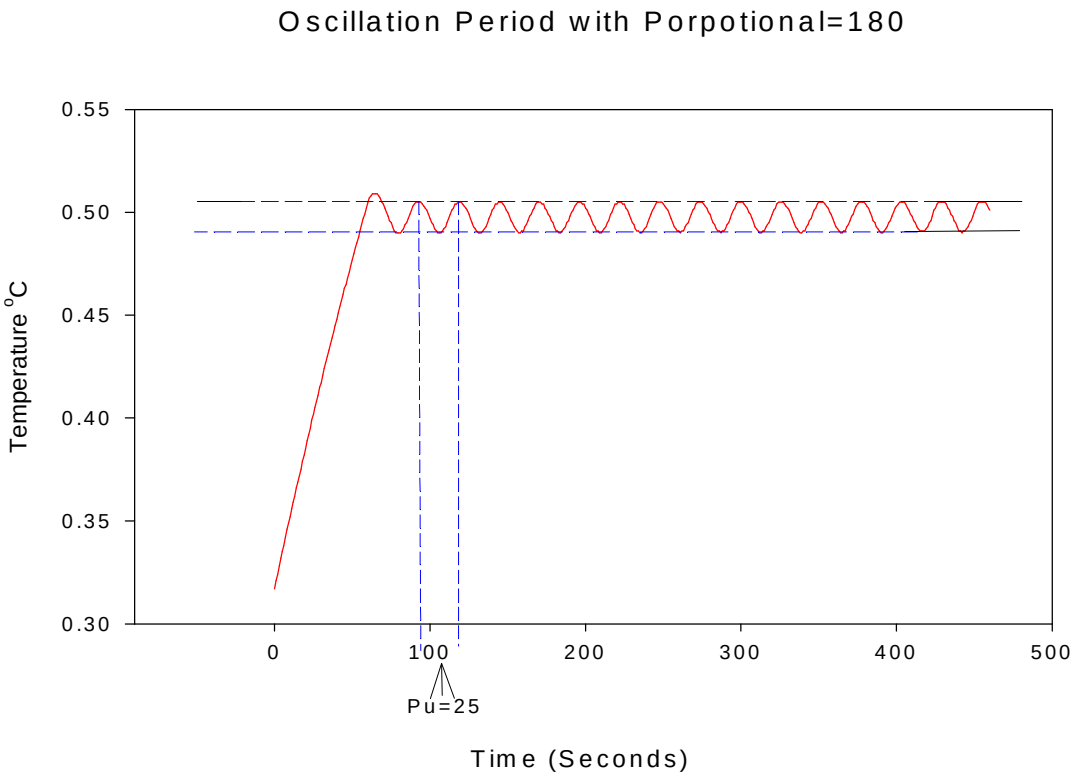

Figure 4.23.: Graph of proportional gain=180 which is also the ultimate gain.

To start with the period of oscillations (Pu) are measured which in this case is 25 seconds as in figure 4.23. The controller parameters are therefore calculated from the following formulas: The following equations are taken from the book Microcontroller Based Temperature Monitoring and Control [21].

$$Kp = 0.6Ku = 0.6 \times 180 = 108$$

$$Ti = Pu/2 = 25/2 = 12.5$$

$$Td = Pu/8 = 25/8 = 3.125$$

Where Kp is the proportional gain, Ku is the ultimate gain, Ti is the integral time, Td is the derivative time and Pu is the oscilation period.

From these parameters the proportional, integral and differential constants can be worked out, which can be put into the digital algorithm, from the following formulas [22].

$$a = Kp = 108$$

$$b = \frac{KpT}{Ti} = \frac{108 \times 1}{12.5} = 8.64$$

$$c = \frac{KpTd}{T} = \frac{108x3.125}{1} = 337$$

Where a is the proportional gain constant, b is the integral gain constant, c is the differential gain constant and T is the sampling period. The a,b and c values can then be put into the digital algorithm specified in the book [23].

These constants were then entered into the system to control the crystal oven and the system response is shown below in figure 4.24. A stepped temperature response with the closed loop parameters is shown in figure 4.25. It can be seen that the response times are very similar to that of the manual tuned responses (figure 4.20 and figure 4.21) however there is a noticeable difference when the temperature gets stepped down from 50 degrees Celsius to 40 degrees Celsius. The fall time in the manual tuning response is 130 seconds and in the closed loop tuned response the settling time is 80 seconds. This indicates significant improvement for required set point changes. Although both tuning methods were suitable for this application the closed parameters were used because of increased speed with regard to set point changes. Also care has to taken when manually tuning a system that it doesn't become unstable.

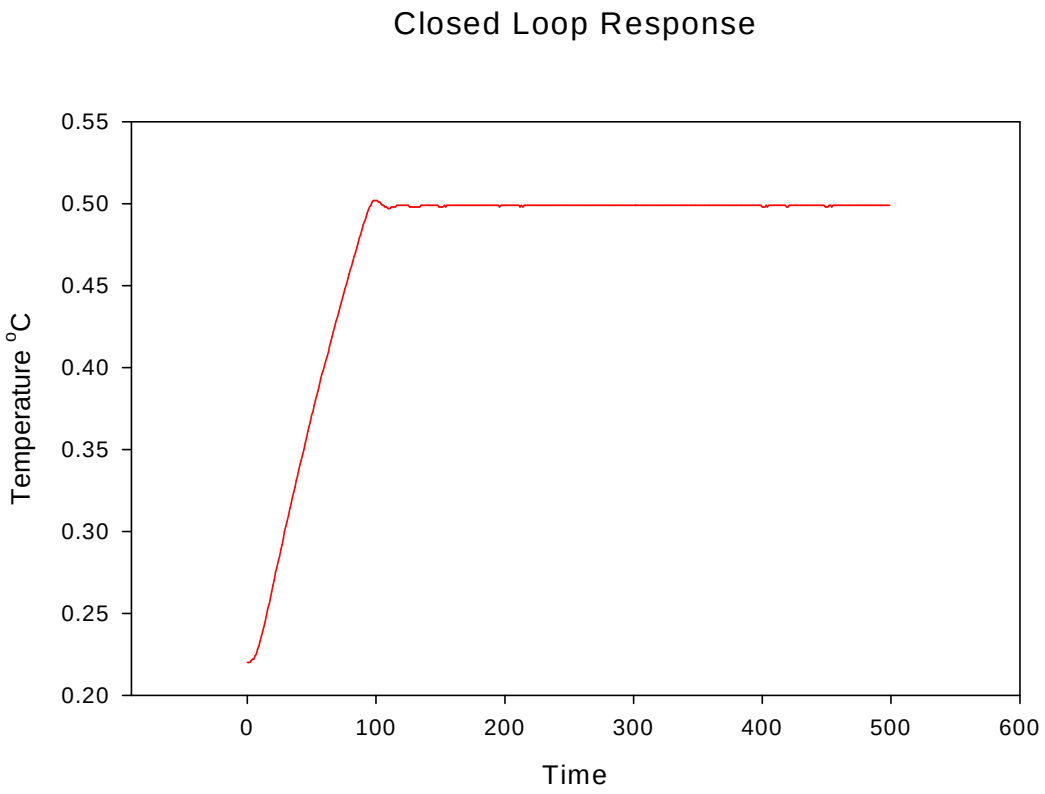

Figure 4.24.: Graph of 'Zeigler Nicholls' closed loop tuned system response

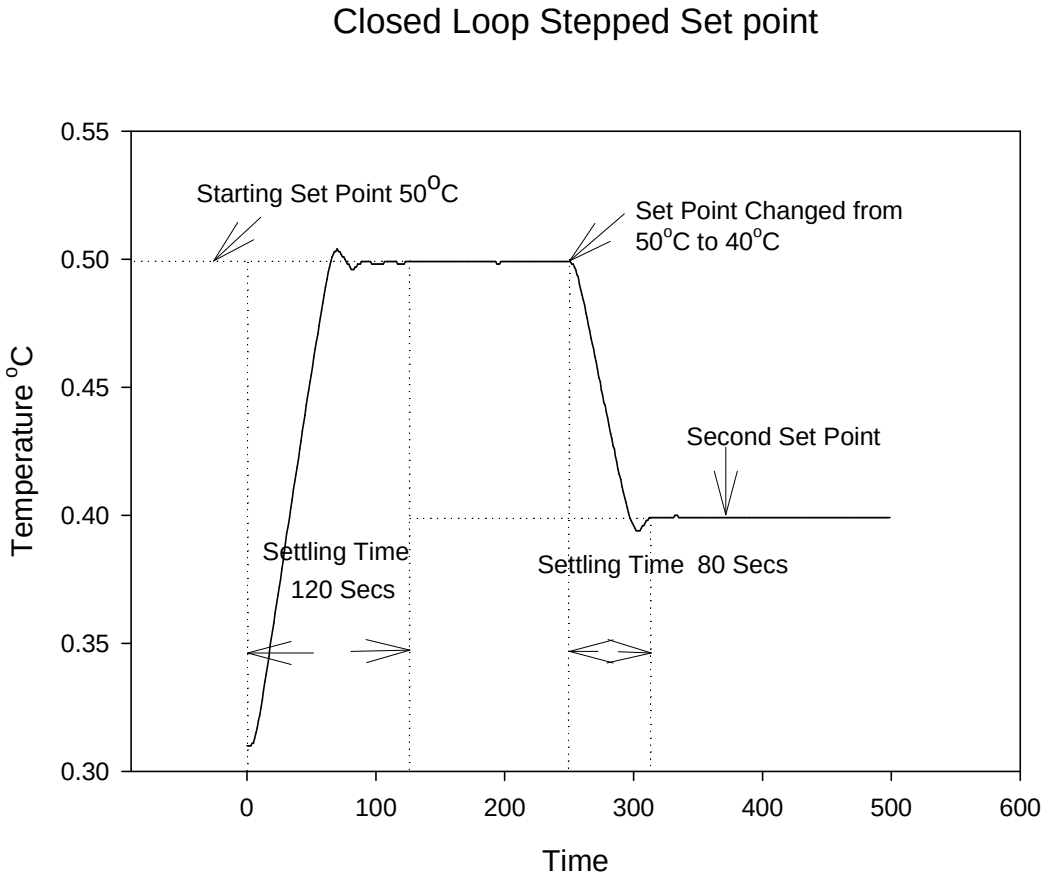

Figure 4.25.: Graph of manually tuned system

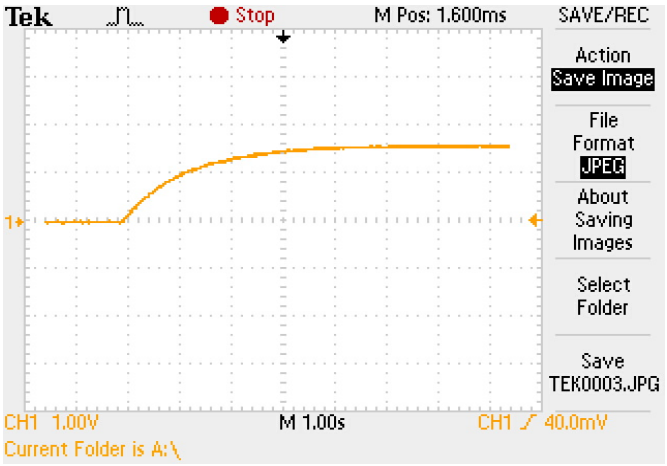

Figure 4.26: Oscilloscope trace of soft start for laser diode.

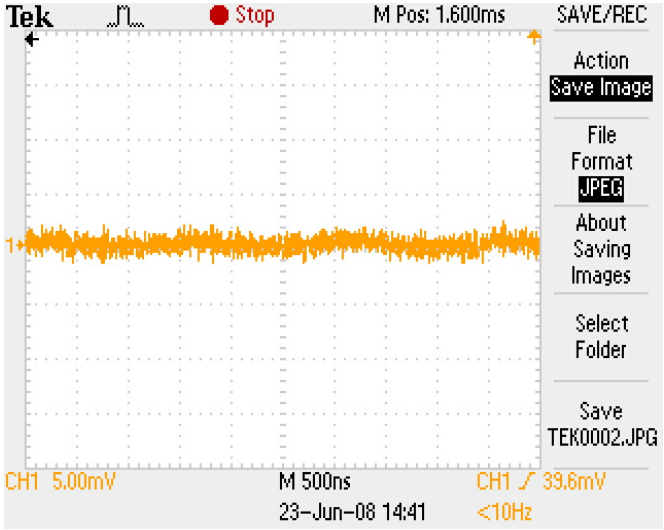

Figure 4.27: Oscilloscope trace of laser diode ripple.

4.9 Summary

Overall, the Laser Management System worked relatively well. The decision to use the PIC18F452 with the embedded HI-TECH C compiler proved a successful choice. To program the firmware in assembly language would have proved tedious and difficult. The time saved and ease of programming in a high level language produced significant results especially in terms of overall development time. The MCU itself was a good choice to be the core of the system. With an instruction cycle of time 100 ns this proved to be of sufficient speed to control and synchronise the whole system. The use of the latches to expand the output lines worked well with simplistic control of these lines by the MCU. The limitation of one PWM channel on the MCU forced the introduction of another method to be designed to accommodate the temperature control of the two specified channels. This was solved successfully by using two small, less powerful MCU's each with its own PWM output. The data was transmitted by the main MCU to each of the smaller MCU's alternatively to set their corresponding PWM output value which was the input to the TEC drive stage. The TEC drive stages for the laser diode and the non-linear crystal worked extremely well built around the LMD18200T H-bridge device. With only the PWM input from the small MCU devices and a direction input allowing current to flow in both directions though the TEC device, the H-bridge device operates in a very simplistic manner reducing increased overheads if this stage was to be designed discretely. Perhaps the weakest part of the system design was that of the Q-switch driver electronics. Although this worked to a fashion it was found out that the minimum pulse width should indeed be 50 ns and not 100 ns as originally thought. With the multivibrator allowing only for a minimum of 100 ns this stage should be redesigned if further development of the system is required. The DAC and the laser diode drive circuitry worked well within the system. The resolution of the DAC allowed for 1mA steps where in fact it was decided that steps of 100mA through the laser diode were more than sufficient and thus the larger step value was implemented into code. The laser diode control circuitry along with the various hardware protection elements to protect the expensive device worked extremely well. Figure 4.26 shows the soft start response (approximately 3 seconds) across the laser diode to help protect the device from sharp transients which in effect could damage the diode. Figure 4.27 shows the ripple on the laser diode when running. The ripple current is 3 mV peak to peak which, being approximately 1 part in 1000, is negligible for required wavelength tolerances. . The Remote Interface Control Board allowed for digital

transmission of temperature data to travel alongside the TEC driver cables and the RF cable from the Q-Switch. Thus, the short analogue run of temperature data from the non-linear crystal oven and the laser diode to the RICB was left unaffected by noise which allowed for +/- 0.025 degrees Celsius thermal control. The additional hardware safety of diodes on the RICB to protect the laser diode was indeed a belts and braces type of approach but justified due to the cost and vulnerability of the laser diode. Figure 4.28 shows the RICB board situated in the laser head. The temperature tuning of the non-linear crystal produced excellent results in both the manual tuning method and the "Ziegler-Nichols" open loop method. The tuning of the laser diode proved equally successful. The responses of both methods for the non-linear crystal oven is shown in figures 4.20 and 4.24. The "Ziegler-Nichols" open loop method was chosen for both temperature control channels as it had proved to be better equipped to change from a higher temperature to a lower temperature, although the rise times of both methods were of a similar nature.

Figure 4.29: Photograph of LMS system along with laser.

Figure 4.28 shows a photograph of the LMS system along with the laser. The instrument has worked well in real life practical circumstances in both lab experiments and indeed in various exhibitions to enable the operation and highlight the unique performance of the OPO laser system designed in St Andrews. Improvements of the LMS system could be implemented in any future re-design if indeed

this was required. Perhaps a higher end PIC MCU with a higher pin count could be used and thus eliminating the need for output expansion via the data latches. The MCU could also have a host universal serial bus (USB) peripheral to allow for setting of parameters by a PC. The addition of a USB link along with flash memory could allow feedback of system performance i.e. temperature responses etc. This could be uploaded to a PC to analyse all sorts of information. The MCU could be chosen that has two independent PWM channels and thus eliminating the use of the two extra low performance MCU's. The Q Switch drive electronics are the main weakness within the current system and should be targeted with priority in any future re-design. They could be improved by using discrete components to allow for a lower minimum pulse width of 50 ns, however, perhaps a much better approach would be the inclusion of complex programmable logic device (CPLD) which could easily produce these pulse widths and indeed much lower pulse widths. The inclusion of a CPLD could ease any I/O pressure incurred on the MCU. Finally, two more major improvements could also be implemented. The flexibility to use a thermistor or the semiconductor temperature sensor currently used. The main advantage of a thermistor compared to the semiconductor sensor is that it has a quicker response to temperature due mostly to its smaller thermal mass. The user could type in thermistor parameters such as the beta value, the thermistor value in ohms etc and the MCU would make the appropriate calculations to optimise the performance of the chosen thermistor. The other change would be instead of connecting a resistor in series with the TEC a MOSFET could be connected with its drain and source in series with the TEC and the user inputs the TEC's parameters and again the MCU calculates the voltage to be dropped across the drain and source and adjusts the MOSFETS gate voltage accordingly via a digital to analogue converter. Electronic design in most cases could always be improved upon and indeed this is the case with the LMS. The design and construction techniques demonstrated with the LMS proved sufficient in its aim of lab experiments and also help show off the portability of the OPO laser system it was intended to drive at various exhibitions around the world. This portability was a major issue as previous OPO systems with matching power and performance were of a much bigger physical size and lacked any sort of portability.

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http://students.creol.ucf.edu/zge/Papers/JDT-WGP.pdf Reflective Mode LCD technology

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AD7391 10-Bit Analogue to Digital Converter

[14] *Roger L. Stevens,* SPI Protocol , Serial PIC'n

[15] *Burr Brown*
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[16] *National Semiconductor*
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LM35DZ Temperature Sensor *Data Sheet*

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[19] *Hi-Tech Software*
http://www.htsoft.com C-Compiler Advertisement

[20] *Lake Shore Cryotronics, Inc*
http://www.lakeshore.com/pdf_files/Appendices/LSTC_appendixF_l.pdf PID control

[21] *Dogan Ibraham,* Microcontroller Based Temperature Monitoring and Control, *page 190*

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[23] *Dogan Ibraham,* Microcontroller Based Temperature Monitoring and Control, *page 218*

Chapter Five – Conclusions

5.1 Introduction

We conclude this dissertation with a brief overview of the work carried out during the research programme, advances of the technology achieved since its conclusion and potential further improvements.

5.2 Background of work

At the beginning of the project, a prototype spectroscopic mid-infrared imaging system had been established which was limited to use within the development laboratory due to its dependence upon commercial laser drive electronics and the requirement for interfacing to a personal computer for image display. The system comprised two key subsystems: a novel broadly tunable, high power and miniature mid-infrared spectroscopic laser illumination source based upon an intracavity OPO, and an electro-mechanical polygon scanner for image acquisition. The work carried out under this research programme, was split between the development of drive electronics for these two key sub systems.

In the first chapter we conducted a brief review of the technology which underpins the research carried out in this programme, namely the production of high power narrow linewidth, broadly tunable mid infrared radiation by means of an intracavity optical parametric oscillator. This approach obviates the need for high power pump lasers required by more traditional extra-cavity pumped OPOs, which therefore results in a very compact and highly efficient device ideal for man portable designs. The intracavity device requires a constant current source for its diode pump, and a dual-channel temperature controller to stabilise the temperature of the diode pump module and nonlinear frequency conversion crystal in order to ensure wavelength stability of the generated mid-infrared radiation. In the laboratory, these tasks were performed by commercial instrumentation but the development of a single, dedicated supervisory unit running from a single 12 V (i.e. battery) power supply was highly desirable in the

context of a portable, stand-alone device, and the development of such a supervisory unit was the subject of chapter four which will be discussed below.

In order to obviate the very high cost of a cryogen-cooled InSb or MCT mid-infrared video camera, an electro-mechanical scanning system based upon a rotating polygonal mirror and reciprocating galvanometer mirror was devised which offered excellent frame rate and resolution at only a fraction of the cost of a camera. With this technique, the collimated mid-infrared idler beam was raster scanned over the scene of interest and an optical pulse was fired from the laser at each pixel point. A portion of the back-scattered light was then recollected by the optical system and focussed down into a single element mid-infrared photodetector, whose output was then sampled digitally and stored for subsequent image display. The scanner had the advantage that every pixel point was illuminated by the full power of the laser and therefore offered a very good signal to noise measurement. The position of the y-galvanometer mirror was controlled by the electronic supervisory system via a DAC and the system was triggered, via the polygon mirror, with a red diode / HeNe laser and Schmitt opto-trigger detector to keep the system in synchronisation.

5.3 Synopsis of work carried out

Of particular importance, in the context of realising a man-portable device, was the need to eliminate the personal computer (used for image display) from the system. This has been the prime objective of the work reported in this thesis. To this end, a stand-alone image acquisition system has been realised which itself comprised two key subsystems: the image acquisition / hardware control electronics and a stand alone LCD module. In chapter 2 we outlined preliminary investigations into LCD drive technology, and implemented a high-end Microchip Technology DSPic to drive the system. It was discovered early on that it was impractical to drive the LCD module directly from the DSPic (or other microprocessor) due to the dynamic nature of the LCD “memory” which needed constant refreshing, therefore placing a prohibitive overhead on processor power. We therefore implemented a dedicated LCD driver chip from EPSON, which included the required video RAM, a simple 8-bit interface to the DSPic and all of the required drive and refresh signals for the LCD module. Also during this chapter, different LCD technologies were evaluated; namely passive (STN) and active (TFT) display

technologies. It was ascertained that in every area, save price, the characteristics of the STN display were inferior to that of the TFT display. The STN display lacked contrast and, crucially, was unable to render rapidly animated graphics (i.e. video) without severe ghosting of the image from one frame to the next. In contrast, the TFT display yielded crisp, high contrast images with virtually no frame to frame ghosting. At only a moderate increase in cost, it was apparent that the TFT display was the technology of choice for this project, and the flexibility of the EPSON LCD driver chip employed meant that both technologies could be rapidly evaluated.

The evaluation system constructed during the work phase outlined in chapter 2 also comprised of analogue and digital I/O in order to interface to control the scanning electro-mechanical hardware. Whilst this circuitry was tested in order to establish correct operation it was not implemented as the evaluation system was also able to mimic the host PC previously used with the scanning controller which was realised previous to the onset of this research project. In this way it was possible to rapidly evaluate LCD modules without having to repeat previous work. It also led to a change in design philosophy whereby a more modular approach was taken to the image acquisition and image display design. It was realised that by separating the two functions into separate modules a stand alone image display module would be realised which had potential utility in a broad range of future applications, not simply limited to this particular mid-infrared imaging system. Such a design approach led to the work carried out in chapter 3.

The work carried out in chapter 3 was therefore split into two parts: the image acquisition electronics and the display module. The image acquisition system previously realised before the onset of this project, whilst functional, had several limitations in terms of speed and flexibility. The board was redesigned with much improved architecture to facilitate faster movement of data between its peripherals, and a larger memory chip used to facilitate image acquisition at higher spatial resolutions. Whereas previously system timings and image resolution changes required reprogramming of the supervisory PIC, in the new design these parameters could be changed in real time thanks to a bank of on board DIP switches. Due to the similarity in functionality of the new design and old, and in order to minimise development time, the same mid-range PIC processor was used to control the board. The removal of the host PC (and concomitant image upload time) led to significant speed increases up to 8

frames / sec over the previous speed of 6 frames / sec. The possibility of replacing the expensive galvanometer (used for y-scan) with a geared stepper motor was investigated. Whilst the electronics proved successful, mechanical backlash within the gearing mechanism meant that proper registration was lost in the vertical plane between successive frames. Whilst it may be possible to replace the galvanometer with a stepper motor / gear box at a later date, this avenue of investigation was not pursued due to the pressures of time.

A fully stand alone LCD module was realised whose interface was "transparent" to the host processor, and which sat in parallel with the on-board RAM chip. The LCD module interface was effectively a cartesian address map (8 bits of x- and y- axis data) and an 8-bit data bus, of which only the upper 6 bits were used yielding a display with 64 shades of grey. Once the address and data bus had been set, the data was clocked into the module on a single *_CS_* pin, therefore mimicking the operation of a RAM chip in write mode. The module utilised a state-of-the-art dsPIC to handle the incoming data from the interface and manipulate it such that it can be fed to the on-board LCD control chip in the minimum of time. The time taken after taking the clock pin low to a pixel point being displayed was ~5 μs, yielding a maximum frame rate of 13 fps assuming a resolution of 150x100 pixels. The modular nature of the LCD module, coupled with the extremely simple digital interface, meant that the device has great potential to find utility in applications beyond those considered in this thesis.

Finally, the commercial constant current laser diode drive instrumentation and dual-channel temperature controller were replaced with a single, bespoke design which had the ability to be driven from a single rail battery power supply. A high-current op-amp was used in transimpedence mode to generate the constant current, which had a maximum drive ability of 8 A. Many features were added to ensure safe operation of the laser diode; namely soft-start, hard- and software maximum current drive limits, protection diodes in both forward and reverse bias across the laser diode to trap transients and finally short-circuit relays mounted in both the drive electronics and in the laser head. The output stage operated in the conventional transconductance configuration with a low impedence resistor in series with the load (i.e. the diode), across which a constant voltage was maintained in order to effect a constant current.

A simple digitally-based proportional, integral and differential algorithm was developed from the literature in order to realise a dual-channel temperature controller to stabilise the laser diode and nonlinear crystal temperature. The diode temperature was stabilised in order to maximise the overlap between the diode emission wavelength and the peak absorption manifold in the laser gain medium. Since the wavelength of the down-converted illumination radiation is dependent upon the nonlinear crystal temperature, this component was stabilised in order to maintain maximum contrast between the presence and absence of methane in the acquired image. The host PIC microcontroller was programmed in C in order to take advantage of floating point arithmetic, mandated by the PID algorithm. The output to the two peltier controllers was via a highly efficient PWM output stage, each channel being controlled by a direction (i.e. heat / cool) line and an on / off line. In order to minimise the effects of noise, the temperatures of the respective laser diode and nonlinear crystal mounts were digitised by converters within the laser head and transmitted digitally to the host controller. The setpoint temperatures, maximum allowable diode current and PID parameters were stored within the laser head on an electrically erasable programmable read only memory (EEPROM), thereby allowing any particular laser module to be used with any other laser management system. The total current ripple on the laser diode was measured at 3 mA, and the temperatures of the respective optical components was stabilised to within 50 mK, yielding a wavelength stability of 0.02 nm (9.1 GHz) and 0.08 nm (2.2 GHz) from the laser diode and nonlinear crystal, respectively.

5.4 Further work

Since the conclusion of the work outlined in the previous four chapters of this dissertation, some of the technology developed herein has gone on to find application beyond it’s original scope. The mid infrared gas imaging system has been licensed to a commercial laser manufacturing organisation, M Squared lasers Ltd, Glasgow, who have productionised both the opto-mechanical hardware which comprises the laser illumination source and scanning mechanism and the drive elctronics. In their design, the rotating polygon has been replaced by a dual-galvanometer with which to project the mid infrared illumination beam over the scene of interest. The advantage of the dual galvanometer approach over that of the polygon is that the scan can be paused and the beam vectored to any pixel point within the field of view such that stand off spectroscopy can be achieved. In order to maintain registration

between the incoming video data and the position of the illumination beam, the angular position of the x- and y- galvos are sampled in synchronisation with the video detector, the results of which give the correct memory location into which to place the sampled back-scattered illumination data. Clearly, the resulting x- and y- data bytes, and the video data byte, are in the ideal format to be displayed on the stand alone LCD modules developed in chapter 3. Improvements to the design were required as the design as it stood was not fast enough to come with the rate of the incoming data. To this end, the board was redesigned to accommodate a superior dsPIC, the dsPIC33FJ64, allowing the clock rate to be increased from 30 to 40 MIPS. This, along with streamlining of the firmware code (replacing some of the C with in-line assembly language), reduced the pixel refresh period from 6.2 μs to 1.5 μs, a data through put rate of ~670 kHz and allowing a screen refresh rate, at a resolution of 256x240 pixels, of 10.9 fps. As the improved laser illumination source now produced radiation at both the signal and idler wavelengths, thereby enabling simultaneous dual-wavelength scan of the scene via two separate video detectors, two screens were required in order to display the acquired images simultaneously, and a photograph of these appears in figure 5.1. The on-board EPROM was reprogrammed to display the logo of the end-customer, and also to show a graduate grey-scale bar to indicate to the user the tonal range of the displays once in use.

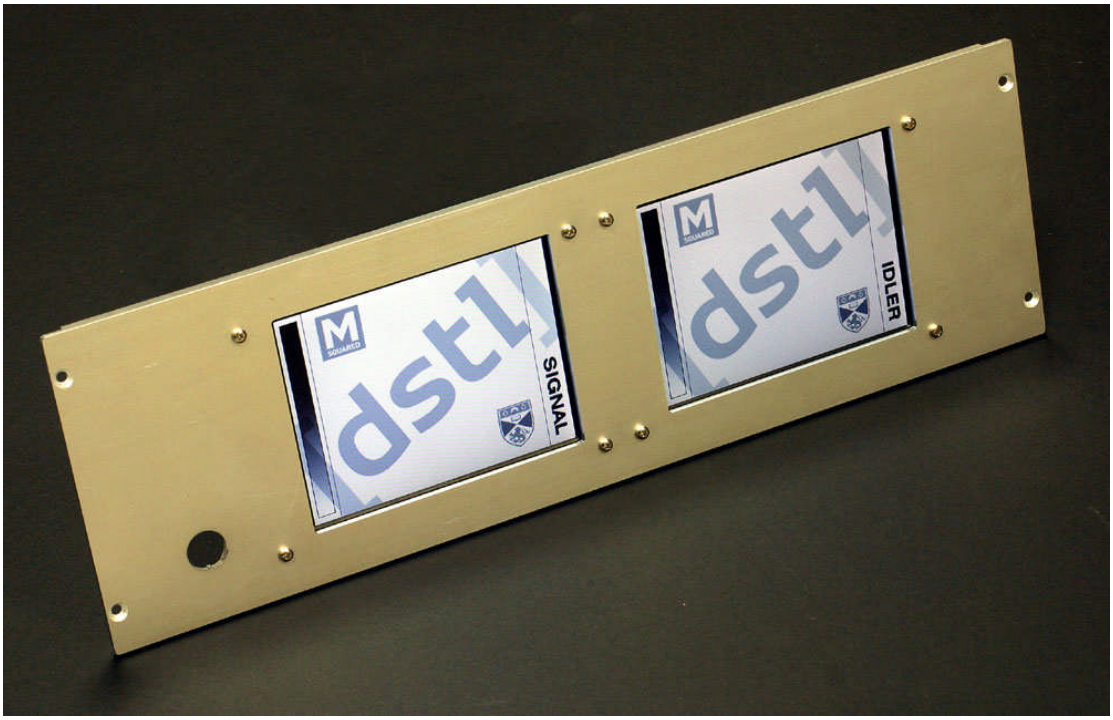

Figure 5.1: Front panel of productionised display module showing LCD screens developed over the course of this research.

Another application which has benefited greatly from the technology developed within this research is the requirement within the departments' research laboratories for an ultra stable temperature controller, used to stabilise the cavity length of an external cavity diode laser system for use in atomic physics [1]. This required the temperature of the device to be stabilised within 5mK and so design improvements over the controller developed in chapter 4 needed to be implemented. Of particular importance was the need to remove the noise caused on the ground line by the high current switching of the PWM output stage. In order to smooth this output without having to resort to more inefficient linear output stage designs, the frequency of the PWM signal was significantly increased to the point to which high current inductors could be placed in series with the TEC load. This greatly reduced both the electromagnetic transmission of noise over the connecting cables and reduced voltage spikes on the controller board. In addition to this, the semiconductor temperature sensor was replaced with a thermistor whose thermal time constant was far less than the semiconductor sensors previously used, which allowed the system to respond more rapidly to temperature fluctuations. In order to use the thermistor, whose response to temperature changes was non linear, the so-called Stein Hart-Hart equation [2] was programmed into the controlling PIC which, once preset with the beta value of the particular thermistor used, could convert back to a Celcius temperature scale.

5.5 Summary

In this dissertation we have presented a number of designs, underpinned by precision digital and analogue techniques, which have enabled a device based upon many years of fundamental laser physics research to be transformed from a laboratory demonstrator into a practical, field operable instrument. By focussing on the end application and requirements, bespoke designs of the laser management system, image acquisition controller and stand alone LCD display module have been realised to maximise the potential utility of the parent technology. The highly modular nature of the approach has meant that the techniques and designs realised over the course of this research have and will continue

to find a variety of use within other fields of research both within the academic and commercial sectors with little or no need for significant further modification.

Chapter 5 References

[1] Paul Zorabedian, “Tunable external-cavity semiconductor lasers,” book chapter in “Tunable lasers handbook”, F. J. Duarte (Ed), Academic Press, 2000.

[2] *Dogan Ibraham*, Microcontroller Based Temperature Monitoring and Control

Appendix A: Project schematic diagrams and printed circuit board (PCB) layouts

The files for all schematic diagrams and printed circuit board layouts are on the digital appendix CD rom in the folder project designs.

These files and the Chapter to which they relate are:
dalc.sch - Chapter 2.
dalc.pcb - Chapter 2.
ral.sch – Chapter 3.
ral.pcb – Chapter 3.
iadd.sch – Chapter 3.
iadd.pcb – Chapter 3.
lms_ricb.sch – Chapter 4.
lms,pcb – Chapter 4.
ricb.pcb – Chapter 4.

The files were generated on Easy-PC and could be viewed with this or compatible software.

Appendix B: Project firmware code

The files for all firmware code are on the digital appendix CD rom in the folder project firmware. The source files and the Projects in which they are situated are set out in chapter numbers. The corresponding .hex files are also situated within the appropriate folders.

The folders are named: Ch2, Ch3 and Ch4.

Open the corresponding project file using the MPLAB integrated development environment (IDE) which is a free download from www.microchip.com

Appendix C: Conference proceedings

C2 – Conference proceedings

1) C. R. Howle, D. J. M. Stothard, C. F. Rae, M. Ross, B. S. Truscott, C. D. Dyer and M. H. Dunn, "Active hyperspectral imaging system for the detection of liquids," Paper 6954-XX, SPIE Chemical, Biological, Radiological, Nuclear, and Explosives (CBRNE) Sensing IX, Orlando, Florida, USA, April 2008.

2) D. J. M. Stothard, C. F. Rae, M. Ross and M. H. Dunn, "Mid-infrared, broadly tunable, active hyperspectral imaging system for the detection of gaseous species," paper 6737-04, SPIE Europe conference on Security and Defence, "Electro-Optical and Infrared Systems: Technology and Applications IV" Florence, Italy, September 2007.

(available on the digital appendix cd under the heading C1_Conference_Proceedings)

3) D. J. M. Stothard, C. F. Rae, M. Ross and M. H. Dunn, "Compact, all solid-state, high repetition rate intracavity optical parametric oscillator and its application to the spectroscopic imaging of gases and liquids," paper CTuU3, Conference on lasers and electro-optics 2007, Baltimore, USA, May 2007.