

Ultracompact all-optical XOR logic gate in a slow-light silicon photonic crystal waveguide

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Abstract: We demonstrate an ultracompact, chip-based, all-optical exclusive-OR (XOR) logic gate via slow-light enhanced four-wave mixing (FWM) in a silicon photonic crystal waveguide (PhCWG). We achieve error-free operation ($<10^{-9}$) for 40 Gbit/s differential phase-shift keying (DPSK) signals with a 2.8 dB power penalty. Slowing the light to $v_g = c/32$ enables a FWM conversion efficiency, η , of -30 dB for a 396 μm device. The nonlinear FWM process is enhanced by 20 dB compared to a relatively fast mode of $v_g = c/5$. The XOR operation requires ≈ 41 mW, corresponding to a switching energy of 1 pJ/bit. We compare the slow-light PhCWG device performance with experimentally demonstrated XOR DPSK logic gates in other platforms and discuss scaling the device operation to higher bit-rates. The ultracompact structure suggests the potential for device integration.

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1. Introduction

All-optical nonlinear signal processing is advancing rapidly, with recent demonstrations of functionalities such as all-optical signal regeneration [1], THz bandwidth multi-impairment monitoring [2], and 1.28 Terabit/s demultiplexing [3]. All-optical logic functions are one of the components expected to compose such a system [4]. To this end, a variety of all-optical logic gates have been demonstrated at speeds up to 640 Gb/s [5]. Research efforts into advanced modulation formats involving phase-encoded signals, such as differential phase-shift keying (DPSK), have received significant attention due to their tolerance to system impairments and nonlinearities [1, 6]. On the device side, all-optical logic functions employing DPSK have been demonstrated in a variety of platforms: highly nonlinear silica fiber (HNLF) [7], semiconductor optical amplifiers (SOAs) [8, 9], and periodically poled lithium niobate (PPLN) [10]. These platforms, however, experience different limitations, including stimulated Brillouin scattering in HNLF, free-carrier patterning effects and a bias current that adds to the energy requirements of SOA, and, in the case of PPLN, temperature control, though a route forward has been suggested [11].

This past year, an all-optical DPSK XOR logic gate up to 160 Gb/s was demonstrated in a 5 cm integrated chalcogenide glass waveguide [12]. The increased nonlinear parameter, γ of integrated waveguides, $\sim 10 \text{ (W-m)}^{-1}$ for chalcogenide and 300 (W-m)^{-1} in silicon nanowires [13], allows for reduced power thresholds to observe a given nonlinear process. Silicon all-optical on-off keying (OOK) logic devices based on micro-ring resonators [14], two-photon absorption [15, 16], or Raman gain [17] phenomena are also capable of low power thresholds, though these devices are limited to bit rates less than 1 Gb/s due to the inherent bandwidth of the resonant structures. This is not an intrinsic limit of silicon, as all-optical functions at much faster rates ($> 1 \text{ Tb/s}$) have been demonstrated [3, 13, 18, 19].

The periodic lattice of the photonic crystal waveguide (PhCWG) gives rise to so-called slow-light effects in which the light travels at a decreased group velocity, v_g , allowing for high intensity light inside the photonic crystal even though small energies are injected. Enhancement of third-order $\chi^{(3)}$ optical processes have been shown to scale as S^2 , where $S = n_g/n_0$ is the ‘slow-down’ factor of the light in the slow medium with group index n_g , and the phase index n_0 [20, 21]. This scaling results from: (i) the increased effective path length of light in the

medium, and (ii) the spatial compression of the pulse intensity in the slow medium, each contributing a factor of S [21–24]. This slow light effect can give rise to nonlinear parameters near $\gamma \sim 10^4$ [25], more than an order of magnitude larger than nanowires made of the same material $\gamma \sim 10^2$. Slow-light enhanced nonlinear processes such as soliton generation [26], self-phase modulation [25,27,28], and third-harmonic generation [29] have been demonstrated in photonic crystal waveguides.

Most recently, four-wave mixing (FWM) in photonic crystals was realized by several groups [30–34], including all-optical demultiplexing of a 160 Gbaud signal in a Si PhCWG [35]. In contrast to the single beam interactions above, slow-light enhances the FWM process as S^4 , though the change in mode area with slow-light must also be taken into account [30, 36]. The development of dispersion engineering in photonic crystals over the past few years has opened the possibility to generate a flat dispersion band of greater than $> \text{THz}$ bandwidth, while simultaneously maintaining slow group velocities [37, 38]. In brief, the slow-light enhancement of optical signals in PhCWGs, combined with broader bandwidth operation provides the means to generate FWM, and therefore all-optical signal processing, over compact $\approx 100 \mu\text{m}$ length scales.

In this paper we demonstrate for the first time, to our knowledge, an all-optical exclusive-OR (XOR) logic gate in photonic crystal waveguides. Our approach employs four-wave mixing (FWM) to perform the logic operation at 40 Gbit/s with return-to-zero (RZ) differential phase-shift keying (DPSK) signals. Slow-light enhancement ($v_g = c/30$) of the optical signal in the photonic crystal waveguide (PhCWG) [9, 12] allows for an ultracompact device ($396 \mu\text{m}$) and suggests potential for integration in future all-optical communication systems.

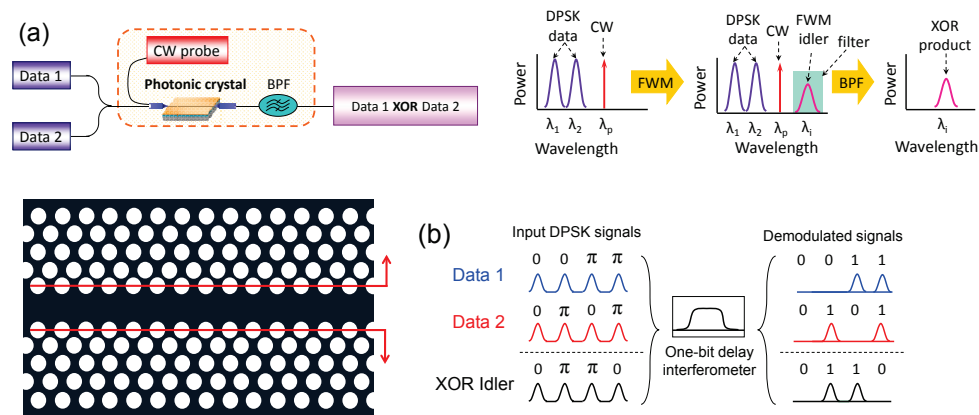


Fig. 1. (a) Schematic of the all-optical XOR logic gate employing non-degenerate four-wave mixing in a dispersion-engineered photonic crystal waveguide (b) Truth table for the XOR logic gate based on DPSK

2. All-optical XOR gate operating principal, sample description, and slow-light four-wave mixing

A schematic of the all-optical XOR logic gate is shown in Fig. 1(a). The all-optical XOR operation arises from non-degenerate four-wave mixing of two phase encoded data signals at λ_1 and λ_2 with a CW probe at λ_p . This generates an XOR output at the idler wavelength λ_i inside the PhCWG. There are in fact three idlers that carry the XOR product [7]. Here we focus on the idler generated by the product of $\omega_i = \omega_2 + \omega_p - \omega_1$. The associated phases of the data channels

therefore mix according to: $\phi_i = \phi_2 + \phi_p - \phi_1$, with the CW signal ϕ_p contributing a constant phase offset between the two data signals. In contrast to the intensity modulation OOK format, the optical signals of DPSK data are encoded with a differential phase of '0' or ' π '. Thus the phase of the generated idler contains the differential '0' or ' π ' states at the output of the XOR gate, with a difference of '0' and ' 2π ' being equivalent. Fig. 1(b) indicates the full truth table of the device, including the output after demodulation in a one-bit-delay interferometer.

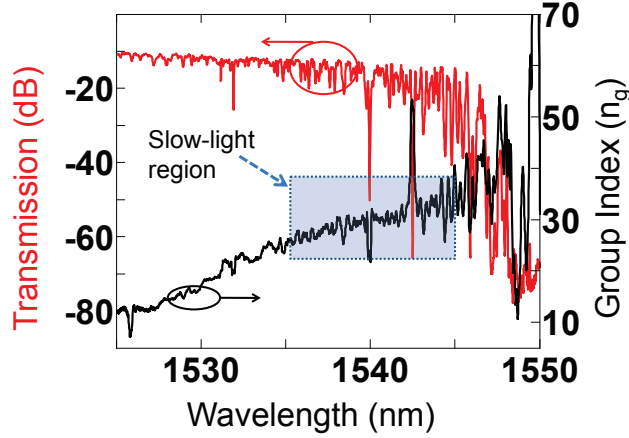


Fig. 2. Measured linear transmission and group index n_g of the sample [30]

The device is a 396 μm long dispersion engineered silicon PhCWG air-suspended structure with a slab thickness of 220 nm, lattice period of 404 nm, hole radii of 115 nm, and first hole lattice shift $s_1 = -50$ nm, similar to that in Ref. [35]. The device includes mode converters to enhance power injection into the device. The adapters include short (100 μm) Si channel waveguide sections, which contribute negligibly to the nonlinear process [30,31]. The photonic crystal region exhibits slow-light enhancement, inducing large intensity in the waveguide allowing for efficient four-wave mixing on a short lengthscale. Fig. 2 shows the measured group index $n_g \sim 30$ covers a 12 nm range centered around 1540 nm, sufficient bandwidth to accommodate the two 40 Gb/s data channels, CW pump signal, and the generated idler. The linear propagation loss in the slow light region was estimated from cutback measurements to be 65 dB/cm [30] with a total insertion loss of -11.8 dB. From the mode area ($A_{eff} \sim 0.5 \mu\text{m}^2$) and the Kerr coefficient $n_2 = 5 \times 10^{18} \text{ m}^2/\text{W}$ of silicon, we estimate the effective nonlinear parameter $\gamma_{eff} \sim \gamma S^2 \sim [2\pi n_2 / \lambda A_{eff}] S^2 \sim 3000 \text{ (W/m)}^{-1}$ for the slow light PhC waveguide [31]. The small change in group-velocity dispersion (GVD), $\beta_2 = -0.6 \times 10^{-21} \text{ s}^2/\text{m}$, over the device bandwidth ensures efficient phase matching of the four-wave mixing process over the device length [30]. The slow-light region is sufficiently flat such that walk-off of the two-pulsed data signals is negligible for this device length. The FWM conversion efficiency, η , in the presence of slow-light and in the undepleted pump approximation, is defined as [31]:

$$\eta = \frac{P_{idler}(L)}{P_{signal}(0)} = S^4 (\gamma P_{pump} L_{eff})^2 \phi e^{-\alpha L}, \quad (1)$$

where $\phi = [\frac{\sinh(gL)}{gL}]^2$, $L_{eff} = (1 - \exp(-\alpha L))/\alpha$, α is the linear loss, and g the parametric gain coefficient as in Ref. [31]. A recent theoretical work derived the effective nonlinear parameters for FWM in photonic crystal waveguides, concluding that the process scales as $S^4 \sim n_{gData1} \times n_{gData2} \times n_{gCW} \times n_{gidler}$ [36], extending prior work on single beam interactions [22]. Though

alluded to for some time in the literature, only this past year was the S^4 scaling experimentally confirmed taking into account the change in mode shape A_{eff} with group index n_g in a single study [30]. In the present device, we thus expect an increase of n_g from 5 to 30 to decrease the device length substantially. A quantitative analysis of the FWM enhancement due to slow light, critical to the short device length in this demonstration, is carried out below in the discussion section.

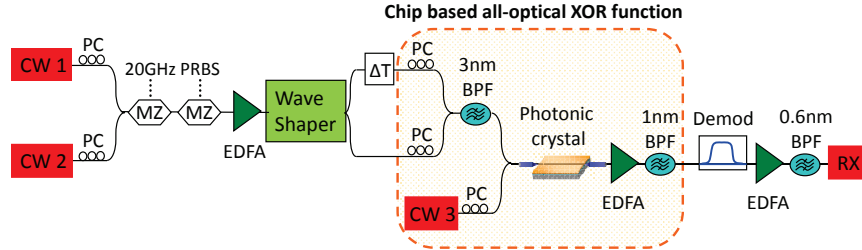


Fig. 3. Experimental setup for the 40 Gbit/s DPSK all-optical XOR logic gate in the compact silicon photonic crystal waveguide

3. Description of experimental setup

Fig. 3 shows the experimental setup. Two 40 Gbit/s RZ-DPSK signals were generated from two CW sources at $\lambda_1=1538.1$ nm and $\lambda_2=1539.5$ nm ($P_{ave} \sim 39$ mW, or ~ 13 mW coupled in the waveguide for each data signal) and a pair of Mach-Zender modulators (MZ). The first MZ carves out the 40 GHz RZ pulses with 33% duty cycle, while the second encodes a 40 Gbit/s pseudorandom bit sequence (PRBS) of 2^7-1 pattern length. The two DPSK signals were amplified, then demultiplexed spectrally in a pulse shaper [39], with one of the branches passing through an optical delay line (ΔT) to separate the signals temporally. These signals are then mixed with the CW pump ($\lambda_p = 1541.7$ nm, $P_{ave} \sim 15$ mW coupled) via a coupler before being sent to the chip. The three signals combined for a total of 41 mW coupled to the waveguide. We measured negligible two-photon absorption in the Si PhCWG at this power level, consistent with our prior measurements [30, 31]. Each channel had a polarization controller to ensure proper alignment to the device transverse-electric mode (TE), e.g. transmission in the plane of the slab. The collected signal is amplified, with the XOR idler then extracted by a 1 nm filter before being demodulated, filtered again to improve the optical signal-to-noise ratio (OSNR), and detected by a 40 Gbit/s receiver.

4. Experimental results

4.1. Role of slow-light enhanced four-wave mixing

Fig. 4 shows the measured output spectrum at the output of the Si PhCWG. The two input 40 Gbit/s DPSK data channels, CW probe signal and the XOR idler generated at $\lambda_i = 1543.0$ nm (shaded region), are indicated. We tuned the CW pump signal over a spectral range of approximately 4.5 nm with flat-top FWM conversion efficiency, Fig. 4 (inset). Including the separation bandwidth of the two data signals here (1.6 nm), this range is in relative agreement with our prior degenerate FWM measurements [30]. The conversion bandwidth offers the potential for wavelength multicasting of the XOR gate [18]. From our experimental parameters, $\phi \approx 1$ and $\gamma_{eff} P_{pump} L_{eff} \approx 0.05$. According to Eqn. 1, the estimated FWM efficiency is $\eta_{theory} = -30$ dB. As the CW is the largest signal, it acts as the pump in this scheme, and we take the data sig-

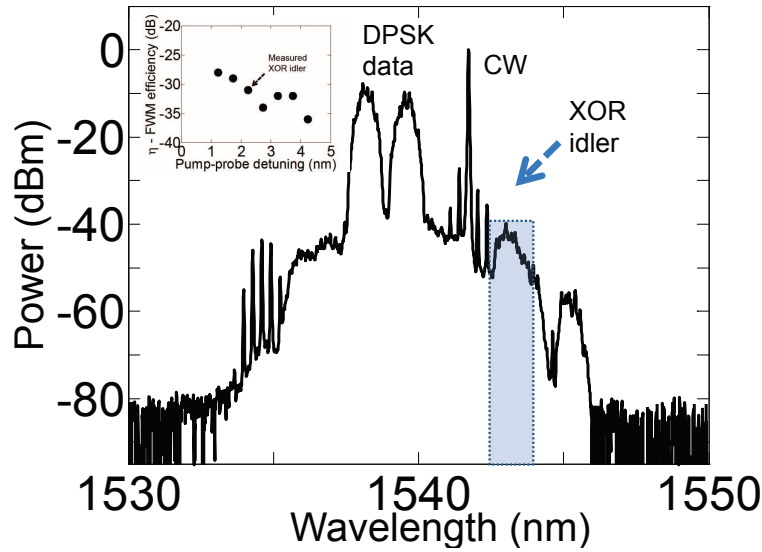


Fig. 4. Four-wave mixing spectra at the output of the chip. The two input data channels, CW probe and generated XOR idler are indicated. Inset: Measured four-wave mixing (FWM) conversion efficiency.

nals as the probe. This yields a measured FWM efficiency of $\eta_{exp} = -30$ to -32 dB, depending on whether Data 1 or Data 2 is the reference signal. The converted idler exhibits some of the structure of the PhCWG transmission, deviating from a smooth curve, due to structural disorder induced during fabrication. Additional discussion of this topic is detailed below.

While γ_{eff} scales as S^2 , it is known that the modal area also increases with group index [27, 31, 36, 40]. In Table 1, we quantify the benefits of slow-light in enhancing the FWM process. We compare the cases of a mode away from the PhC band-edge $n_g = 5$, the sample investigated here $n_g = 30$, and a typical silicon nanowire. While we expect an enhancement of $S^4 \sim 1100$ (30 dB) by going from $n_g = 5$ to 30, the increased mode area reduces the enhancement by about 8 dB, with loss accounting for an additional 2 dB. The result is a 20 dB enhancement of the FWM process employing a slow-light mode ($n_g = 30$) versus a relatively fast mode ($n_g = 5$). The FWM conversion efficiency, η , is the critical parameter to achieve the logic operation. If we desire a conversion efficiency of $\eta = -30$ dB at a fixed input power of $P_o = 40$ mW, we observe the photonic crystal achieves the desired operation at 7.5 times shorter device compared to a silicon nanowire, demonstrating the ability of slow-light to greatly enhance nonlinear interactions.

Table 1. Quantitative enhancement of four-wave mixing due to slow-light. $P_o = 40$ mW.

Platform	n_g [-]	A_{eff} [μm^2]	S [-]	α [dB/cm]	Length [μm]	η [dB]
Si nanowire	5	0.15	1.5	3	3×10^3	-30
Si PhCWG	5	0.2	1.5	10	400	-50
Si PhCWG	30	0.5	8.7	65	400	-30

4.2. DPSK XOR logic gate results

Figure 5(a) shows the demodulated temporal waveforms captured on a sampling oscilloscope of the two input data and output XOR channels. One can see the FWM idler is the XOR output from the two input DPSK channels, confirming the all-optical logic gate functionality. The eye diagrams of the 40 Gbit/s signals after the chip and demodulation are seen in Fig. 5(b). While the eyes of the data signals are relatively crisp, the XOR product is noisier due to the small energy of the idler coming from the photonic chip. The 396 μm device achieves the XOR operation at estimated energy of ~ 1 pJ/bit, including all signal beams.

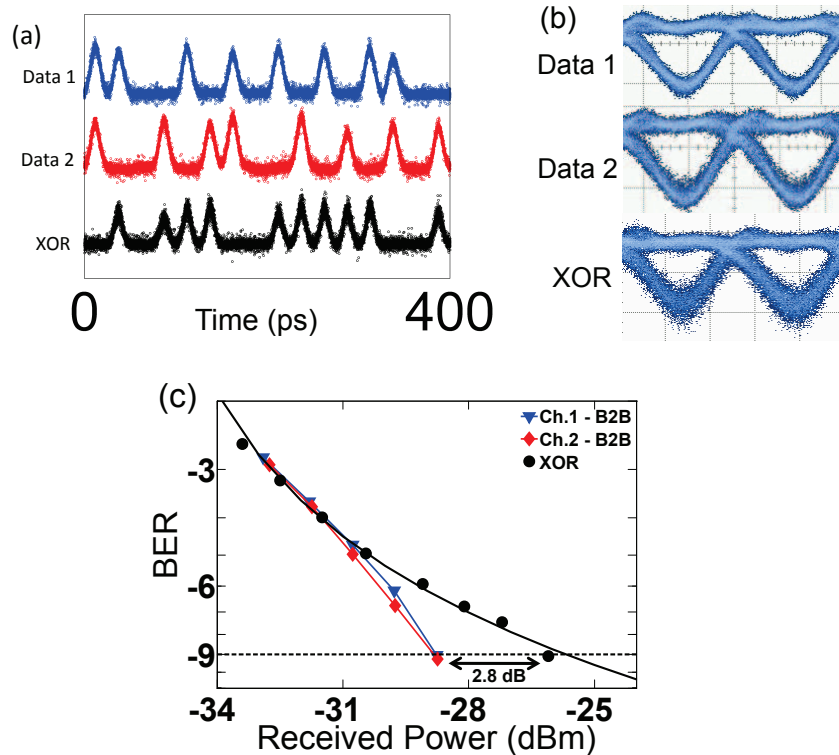


Fig. 5. (a) Temporal waveforms of the two input data channels and output XOR idler. (b) Eye diagrams of the respective channels. (c) Bit-error rate measurements of the various data 40 Gb/s DPSK signals. The device is error free ($\text{BER} < 10^{-9}$) with ~ 2.8 dB power penalty, primarily attributed to the small signal amplified off-chip.

We next performed bit-error-rate (BER) measurements, Fig. 5(c), observing 'error-free' ($\text{BER} < 10^{-9}$) operation for the all-optical XOR logic gate. The generated XOR product experienced a power penalty of ~ 2.8 dB compared to the back-to-back case, which included a single amplification stage. Though the origin of the power penalty is unclear, there are a few possible processes that could contribute. First, the amplification of the small signal required to generate the idler in our nanophotonic device is a possible source of power penalty. As collecting the light off chip is the largest source of loss, one can presume a smaller power penalty if the output were employed directly in other on-chip functions, as envisioned in future photonic integrated circuits. Second, some disorder in the regular photonic lattice could also contribute phase differences as the light propagates along the waveguide. A third solution is to generate

additional idler (XOR) signal in the FWM process. This could be achieved by injecting more power, or improving the device fabrication to reduce scattering losses. Improved photonic crystal fabrication is an extremely active area of research that would help with the second and third points. In addition to technological improvements in lithography and etching techniques, newly proposed approaches to reduce loss via precise control of hole-hole scattering coherence and mode shape have only recently been explored [41]. The 'loss engineering' of Ref. [41] is expected to improve PhC devices even with current fabrication technologies. We now compare the slow-light photonic crystal XOR DPSK logic gate performance to other demonstrations.

5. Discussion

All-optical XOR gates have been demonstrated in a variety of platforms. We focus here on DPSK results for the reasons we mentioned in the introduction, namely robustness against system impairments. The key parameters of the devices are listed in Table 2. These include: length, experimental bit rate, energy per bit (P_{avg} / bit-rate), bit-error rate results (if provided), and the nonlinear conversion efficiency. For this section we use the instantaneous FWM efficiency, $\eta_o = \frac{P_{idler}(L)}{P_{signal}(L)}$, since the input power values of several systems are not readily available. The output optical spectrum is presented, however, and allows direct comparison. We ignore external amplifiers in all cases and focus solely on the FWM process in the energy calculation. Note that the electrical power required for SOAs is not taken into consideration in this estimate [42]. All of the demonstrations thus far have been based on four-wave mixing, with the exception of PPLN [10] which is based on sum-frequency generation, where we define the conversion efficiency as η_1 .

Table 2. Comparison of experimentally demonstrated exclusive-OR (XOR) logic gates

Platform	Length [mm]	Bit rate [Gb/s]	Energy [pJ/bit]	BER results [dB/pattern]	η_o [dB]
SOA [8]	2.6	40	0.6 ⁺	N/A	-35
SOA [9]	—	10	0.1 ⁺	0 dB / $2^{31} - 1$	-20
PPLN [10]	50	40	0.125**	N/A	$\eta_1 = -40$
HNLFF [7]	1.35×10^5	40	0.1**	N/A	-20
Chalcogenide [12]	68	40	0.75	0 dB / $2^7 - 1$	-45
(As ₂ S ₃)		160	0.187	N/A	-57
Si nanowire [43]	5	40	0.675	4 dB / $2^7 - 1$	-25
Si PhCWG (here)	0.4	40	1	2.8 dB / $2^7 - 1$	-30

⁺ This does not include the electrical energy which would dominate the optical energy in these devices.

** Injected energy is not included in the original paper. We thus estimated these values from the output OSA trace and linear loss, if given.

The Si PhCWG XOR operation presented here compares favorably well across a broad range of categories, the most salient advantage being nearly an order of magnitude shorter device length ($\sim 400 \mu\text{m}$) and the most notable drawback being bandwidth ($\sim 1 \text{ THz}$). This tradeoff is well-documented in the PhC literature [20, 21, 38]. This bandwidth however, is capable of performing the 40 Gb/s XOR logic operation here, and other all-optical signal operations, such as optical signal to noise ratio (OSNR) monitoring, up to 640 Gb/s [19]. The energy consumption of the device is close to its integrated counterparts (Si and ChG), with expected parity due to improved fabrication [41]. Though XOR logic gates have been demonstrated qualitatively in

a number of platforms, relatively few have measured the bit-error rate (BER) of the operation. The best reported BER results are in ChG waveguides and SOAs, though the latter was at 10 Gb/s. The measured power penalty of the PhCWG in this work could be improved as noted in the BER measurements above. The ChG experiment also included a demonstration at 160 Gb/s, though no BER was measured in that case. We note that 640 Gb/s XOR logic has been demonstrated with OOK [5].

We conclude with a few statements on scaling the device to higher baud-rates (>100 Gb/s). Photonic crystal waveguides exhibit a well known tradeoff between the group index and bandwidth, commonly called the group index-bandwidth product (GBP) [38]. The broader bandwidth of a 160 Gb/s XOR logic gate would thus require a device with a smaller group index, e.g. $n_g = 24$. Taking into account the smaller mode size and decreased linear scattering loss at this faster group velocity, we estimate a device length of $600\text{ }\mu\text{m}$ would be required to achieve the same FWM efficiency, $\eta = -30$ dB. All-optical XOR operation at even higher bit-rates is possible with dispersion management of shorter temporal signals and careful design of the group index-bandwidth properties.

6. Conclusion

We have demonstrated an ultra-compact all-optical XOR gate using non-degenerate four-wave mixing in a dispersion-engineered photonic crystal waveguide for 40 Gbit/s DPSK signals. Error-free XOR operation was achieved with a 2.8 dB power penalty. Slowing the optical signals to velocities of $\sim c/30$ enhance the nonlinear process by 20 dB, allowing for the operation in a $396\text{ }\mu\text{m}$ long device, approximately an order of magnitude shorter than prior demonstrations. Compact device operation suggests the potential for integration on an integrated photonic chip. The device operation is scalable to increased baud rates in slow light structures with increased bandwidth.

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